



SREE RAMA ENGINEERING COLLEGE

(AUTONOMOUS)

Approved by AICTE, New Delhi – Affiliated to JNTUA, Ananthapuramu
 Accredited by NAAC with 'A' Grade
 Rami Reddy Nagar, Karakambadi road, Tirupati-517507

Department of Electronics and Communication Engineering

SRET25 M. Tech VLSID

Course Structure

Semester-I						
S. No.	Course Code	Course Name	L	T	P	Credits
1.	25MTVD01T	CMOS Analog IC Design	3	0	0	3
2.	25MTVD02T	CMOS Digital IC Design	3	0	0	3
Program Elective – I						
3.	25MTVD03Ta	Microchip Fabrication Techniques	3	0	0	3
	25MTVD03Tb	Scripting Languages for VLSI				
	25MTVD03Tc	CAD for VLSI				
Program Elective – II						
4.	25MTVD04Ta	Device Modelling	3	0	0	3
	25MTVD04Tb	FPGA Architectures and Applications				
	25MTVD04Tc	ASIC Design				
5.	25MTVD01P	CMOS Analog IC Design Lab	0	0	4	2
6.	25MTVD02P	CMOS Digital IC Design Lab	0	0	4	2
7.	25MTMB01T	Research Methodology and IPR	2	0	0	2
8.	25MTVD01S	RTL Synthesis Simulation and verification	0	1	2	2
Audit Course – I						
9.	25MTHS01Aa	English for Research paper writing	2	0	0	0
	25MTSE01A	Disaster Management				
	25MTHS01Ab	Essence of Indian Traditional Knowledge				
Total			16	1	10	20

M. Tech. VLSID
I Year – I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

(25MTVD01T) CMOS ANALOG IC DESIGN
(VLSID)

Course Objectives:

This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies, Basic design concepts, issues and tradeoffs involved in analog IC design are explored, Intuitive understanding and real-life applications are emphasized throughout the course, Design of CMOS Op Amps, Compensation of Op Amps, Design of Two- Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp and Characterization of Comparator, Two-Stage, Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators etc.

Course Outcomes (CO): On completion of the course, the student should be able to

- CO1. Understand MOSFET based analog integrated circuits. (L2)
- CO2. Analyze Differential pairs and current mirror circuits (L4)
- CO3. Understand and appreciate the importance of noise and distortion in analog circuits. (L2)
- CO4. Design the feedback amplifiers with op-amps (L5)
- CO5. Understand open loop comparator's and its types (L2)

UNIT - I: Basic MOS Device Physics

No. of Hours - 10

General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models and MOS Capacitor. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

UNIT - II: Differential Amplifiers

No. of Hours - 10

Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. Current Steering Circuit

UNIT – III: Frequency Response of Amplifiers

No. of Hours - 10

General Considerations, Common Source Stage, Source Followers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

UNIT – IV: Feedback Amplifiers:

No. of Hours - 10

General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps, Stability and Frequency Compensation.

UNIT – V: Comparators:

No. of Hours - 10

Characterization of comparator, Two-Stage, Open-Loop comparators, Other Open- Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

Textbooks:

1. B. Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition, 2016.
2. Paul. R.Gray& Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009.

Reference Books:

1. T.C.Carusone, D.A.Johns & K.Martin, "Analog Integrated Circuit Design", 2nd Edition, Wiley, 2012.
2. P.E.Allen & D.R.Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.
3. R.Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, Wiley, 2010.
4. Adel S. Sedra, Kenneth C. Smith, Arun, "Microelectronic Circuits", 6th Edition, Oxford University Press.

M. Tech. VLSID
I Year– I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

(25MTVD02T) CMOS DIGITAL IC DESIGN
(VLSID)

Course Objectives:

- To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
- The course also involves analysis of performance metrics.
- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

Course Outcomes: On completion of the course, the student should be able to:

- CO1. Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS. (L2)
- CO2. Analyze, design and implement Combinational MOS Logic Circuits (L4)
- CO3. Analyze, design and implement Sequential MOS Logic Circuits (L4)
- CO4. Understand the basic principles and operation of dynamic logic circuits, design high-speed dynamic CMOS logic gates using transmission gates. (L2)
- CO5. Classify different types of semiconductor memories. (L3)

UNIT I: MOS Design Pseudo NMOS Logic

No. of Hours: 12

Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic

UNIT II: Combinational MOS Logic Circuits

No. of Hours: 10

MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT III: Sequential MOS Logic Circuits:

No. of Hours: 08

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

UNIT IV: Dynamic Logic Circuits:

No. of Hours: 10

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT V: Semiconductor Memories

No. of Hours: 10

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Textbooks:

1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.

3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, AnanthaChandrakasan, Borivoje Nikolic, 2ndEdition, PHI.

M. Tech. VLSID
I Year - I Semester

SRET25 Regulations

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3	0	0	3

**(25MTVD03Ta) MICROCHIP FABRICATION TECHNIQUES
(VLSID)**

Program Elective - I

Course Objectives:

The course aims to introduce students to semiconductor manufacturing processes, including wafer fabrication, photolithography, doping, and metallization and understand the principles and techniques involved in fabricating semiconductor devices and analyze the factors affecting yield and reliability

Course Outcomes: On completion of the course, the student should be able to:

- CO1. Understand the basics of semiconductor industry and wafer fabrication operations (L2)
- CO2. Explain the photolithography process, including oxidation, patterning, and etching techniques. (L1)
- CO3. Understand and differentiate various doping and deposition processes, including diffusion and ion implantation to evaluate their impact on semiconductor device performance. (L2)
- CO4. Apply understanding of metallization and film deposition techniques, including CVD and epitaxy, to design and optimize semiconductor fabrication processes. (L3)
- CO5. Analyze design rules and scaling for BICMOS ICs, and packaging technologies. (L4)

UNIT I: Introduction to processing

No. of Hours: 11

Overview of semiconductor industry, Stages of Manufacturing, Process and product trends, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Yield measurement, Contamination sources, Clean room construction.

UNIT II: Photo-lithography

No. of Hours: 10

Oxidation and Photolithography, Ten step patterning process, Photoresists, physical properties of photoresists, Storage and control of photoresists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping

UNIT III: Diffusion and Ion implantation

No. of Hours: 09

Doping and depositions: Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2.

UNIT IV: Film deposition and Growth

No. of Hours: 10

Metallization, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT V:

No. of Hours: 12

Yield: Design rules and Scaling, BICMOS ICs: Choice of transistor types, PNP transistors, Resistors, capacitors.

Packaging: Chip characteristics, package functions, package operations.

TEXT BOOKS:

1. Peter Van Zant, Microchip fabrication, McGraw Hill, 1997.
2. Plummer, J.D., Deal, M.D. and Griffin, P.B., "Silicon VLSI Technology: Fundamentals, Practice and Modeling", 3rd Ed., Prentice-Hall, 2000.

REFERENCE BOOKS:

1. C.Y. Chang and S.M. Sze, ULSI technology, McGraw Hill, 2000
2. S.K. Gandhi, VLSI Fabrication principles, John Wiley and Sons, NY, 1994
3. S.M. Sze, VLSI technology, McGraw-Hill Book company, NY, 1988

M. Tech. VLSID
I Year - I Semester

SRET25 Regulations

L	T	P	C
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**(25MTVD03Tb) SCRIPTING LANGUAGES FOR VLSI
(VLSID)**

Program Elective - I

Course Objectives:

- Learn programming with scripting languages
- Understand how to create and run scripts using PERL/TCL/PYTHON in CAD Tools
- Gain knowledge about PERL/PYTHON/ TCL in developing system and web applications
- Develop skill to design a real time project using PERL/PYTHON

Course Outcomes: On completion of the course, the student should be able to:

- CO1. Understand the fundamental concepts of scripting languages, their characteristics, and applications in modern computing environments. (L2)
- CO2. Develop basic PERL scripts using variables, control structures, arrays, hashes, I/O operations, and regular expressions to solve simple automation tasks. (L3)
- CO3. Apply advanced PERL features such as references, modules, file handling, objects, and system interaction to create modular and secure scripts. (L4)
- CO4. Develop TCL programs using its syntax, control flow, procedures, data handling, string manipulation, and file operations for scripting-based applications (L3)
- CO5. Develop advanced TCL scripts and Python programs using namespaces, libraries, events, exceptions, built-in methods, and module integration for real-time and internet-aware applications. (L4)

UNIT - I: Introduction to Scripting Languages

No. of Hours: 10

Introduction to Scripts and Scripting: Basics of Linux, Origin of Scripting languages, scripting today, Characteristics and uses of scripting languages.

UNIT – II: Fundamentals of PERL Programming

No. of Hours: 10

PERL: Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

UNIT – III: Advanced PERL Concepts and Applications

No. of Hours: 10

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, working with files, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects and modules in action, Tied variables, interfacing to the operating systems, Security issues.

UNIT – IV: Basics of TCL Programming

No. of Hours: 10

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

UNIT – V: Advanced TCL Features and Introduction to

No. of Hours: 10

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, TCL and TK integration.

PYTHON: Introduction to PYTHON language, PYTHON-syntax, statements, functions, Built-in functions and Methods, Modules in PYTHON, Exception Handling.

Textbooks:

1. The World of Scripting Languages- David Barron, Wiley Student Edition.
2. PYTHON Web Programming, Steve Holden and David Beazley, New Riders Publications.

Reference Books:

1. TCL/TK: A Developer's Guide- ClifFlynt, Morgan Kaufmann Series.
2. Core PYTHON Programming, Chun, Pearson Education.
3. Learning Perl, Randal L. Schwartz, O' Reilly publications 6th edition.
4. Linux: The Complete Reference", Richard Peterson McGraw Hill Publications, 6th Edition.

M. Tech. VLSID
I Year - I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

**(25MTVD03Tc) CAD FOR VLSI
(VLSID)**

Program Elective - I

Course Objectives:

To understand the various phases of CAD for digital electronic systems, from digital logic simulation to physical design, including test and verification, understanding of fundamental concepts in CAD and to establish capability for CAD tool development and enhancement, fundamentals of VLSI technologies and optimization of design for area, timing and power by applying suitable constraints.

Course Outcomes (CO): Student will be able to

- CO1. Understand VLSI and Physical Design cycles, various design and System packaging styles. (L2)
- CO2. Understand about partitioning, Pin Assignment, Placement and analyze various partitioning algorithms and Simulated annealing. (L2)
- CO3. Analyze various floor planning and Pin assignment algorithms. (L4)
- CO4. Analyze various Placement and Routing algorithms. (L4)
- CO5. Understand Physical design cycles of FPGAs and MCMs, partitioning and Routing of FPGAs (L2)

UNIT – I : Introduction

No. of Hours - 10

VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT – II : Partitioning

No. of Hours - 10

Partitioning, Pin Assignment and Placement: Partitioning – Problem formulation, Classification of Partitioning algorithms, Kernighan-Lin Algorithm, Simulated Annealing.

UNIT – III : Floor Planning

No. of Hours - 10

Problem formulation, Classification of floor planning algorithms, constraint based floor planning, Rectangular Floor Planning: Dualization, Pin Assignment – Problem formulation, Classification of pin assignment algorithms, General and channel Pin assignments.

UNIT – IV : Placement and Routing

No. of Hours - 10

Placement–Problem formulation, Classification of placement algorithms, Partitioning based placement algorithms.

Global Routing and Detailed Routing: Global Routing – Problem formulation, Classification of global routing algorithms, Maze routing algorithms, Detailed Routing – Problem formulation, Classification of routing algorithms, Single layer routing algorithms.

UNIT – V : Physical Design Automation of FPGAs and MCMs

No. of Hours - 10

FPGA Technologies, Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing, algorithms for the Segmented Model; Introduction to MCM Technologies, MCM Physical Design Cycle.

Textbooks:

1. Algorithms for VLSI Physical Design Automation by Naveed Shervani, 3rd Edition, 2005, Springer International Edition.
2. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Ed., 2011.

Reference Books:

1. VLSI Physical Design Automation-Theory and Practice by Sadiq M Sait, Habib Youssef, World Scientific.
2. Algorithms for VLSI Design Automation, S. H. Gerez, 1999, Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd.
3. VLSI Physical Design Automation by Sung Kyu Lim, Springer International Edition.

M. Tech. VLSID
I Year - I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

(25MTVD04Ta) DEVICE MODELLING
(VLSID)

Program Elective - II

Course Objectives:

To acquire knowledge about threshold voltage modelling of 2-terminal MOS device, C-V characteristics of MOSFET, I-V characteristics of 4-terminal MOSFET, and modelling of SOI MOSFETS.

Course Outcomes: on completion of the course, the student should be able to:

- CO1. Understand threshold voltage modelling of 2-terminal MOS device (L2)
- CO2. Analyze the C-V characteristics of MOSFET (L4)
- CO3. Model the I-V characteristics of 4-terminal MOSFET (L4)
- CO4. Analyze small signal analysis of MOSFETS (L4)
- CO5. Understand basic structure and modelling of SOI MOSFET. (L2)

UNIT – I : Threshold Voltage Modeling of 2-Terminal MOS Devices **No. of Hours: 10**

2-terminal MOS device: threshold voltage modelling (ideal case as well as considering the effects of, Φ_{ms} and Dit).

UNIT – II : C–V Characteristics and Applications of MOS Capacitor. **No. of Hours: 10**

C-V characteristics (ideal case as well as taking into account the effects of Q_f , Φ_{ms} and Dit); MOS capacitor as a diagnostic tool (measurement of non-uniform doping profile, estimation of Q_f , Φ_{ms} and Dit)

UNIT – III : Threshold Voltage and I–V Modeling of 4-Terminal MOSFETs **No. of Hours: 10**

4-terminal MOSFET: threshold voltage (considering the substrate bias); above threshold I-V modelling (SPICE level 1,2,3 and 4).

UNIT – IV : Small-Signal Analysis of MOSFET **No. of Hours: 10**

Sub threshold current model; scaling; effect of threshold tailoring implant (analytical modelling of threshold voltage using box approximation); buried channel MOSFET. Short channel, DIBL and narrow width effects; small signal analysis of MOSFETs (Meyer's model).

UNIT V: Advanced MOS Devices **No. of Hours: 10**

SOI MOSFET: Basic structure; threshold voltage modelling Advanced topics: hot carriers in channel; EEPROMs; CCDs; High-K gate dielectrics.

Textbooks:

1. S. M. Sze, Physics of Semiconductor Devices, (2e), Wiley Eastern, 1981.
2. M. Lundstrom, Fundamentals of Nano transistors, World Scientific Publishing Co Pte Ltd., 2017.

Reference Books:

1. Y. P. Tsividis, Operation and Modelling of the MOS Transistor, McGraw-Hill, 1987.
2. E. Takeda, Hot-carrier Effects in MOS Transistors, Academic Press, 1995.
3. J. P. Colinge, "FinFETs and Other Multi-Gate Transistors," Springer. 2009.

M. Tech. VLSID
I Year - I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

(25MTVD04Tb) FPGA ARCHITECTURES AND APPLICATIONS
(VLSID)
Program Elective - II

Course Objectives:

To acquire knowledge about various architectures and device technologies of PLD's, FPGA Architectures, System level Design and their application for Combinational and Sequential Circuits, Anti-Fuse Programmed FPGAs and for various design applications.

Course Outcomes: On completion of the course, the student should be able to:

- CO1. Acquire knowledge about various architectures and device technologies of PLD's (L2)
- CO2. Analyze FPGA Architectures (L4)
- CO3. Analyze System level Design and their application for Combinational and Sequential Circuits (L4)
- CO4. Familiarize with Anti-Fuse Programmed FPGAs (L2)
- CO5. Apply knowledge of this subject and design various applications. (L3)

UNIT – I : Introduction to Programmable Logic Devices

No. of Hours: 10

Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT – II : Field Programmable Gate Arrays

No. of Hours: 10

Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs

UNIT – III : SRAM Programmable FPGAs

No. of Hours: 10

Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures

UNIT – IV : Anti-Fuse Programmed FPGAs

No. of Hours: 10

Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT V: Design Applications

No. of Hours: 10

General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

Textbooks:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition
2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.

Reference Books:

1. Field Programmable Gate Arrays-John V.Oldfield, Richard C.Dorf, Wiley India

2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier, Newnes
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series

M. Tech. VLSID
I Year - I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

(25MTVD04Tc) ASIC DESIGN
(VLSID)
Program Elective - II

Course Objectives:

To understand different types of ASICs and their libraries. Programmable ASICs, I/O modules and their interconnects. To familiarize different methods of software ASIC design their simulation, testing and construction of ASICs.

Course Outcomes: On completion of the course, the student should be able to:

- CO1. Understand different types of ASICs and their libraries. (L2)
- CO2. Explain programmable ASICs, I/O modules, and interconnects. (L2)
- CO3. Demonstrate software ASIC design, simulation, and testing. (L3)
- CO4. Apply HDL-based design and synthesis methods. (L3)
- CO5. Evaluate ASIC construction and testing techniques. (L5)

UNIT – I: ASIC Fundamentals and Cell Library Design

No. of Hours: 10

Introduction to ASICs: Types of ASICs, Design Flow, Case Study, Economics of ASICs, ASIC Cell Libraries, Transistors as resistors, Transistor Parasitic Capacitance, Logical Effort, Library Cell Design, Library Architecture, Gate-Array Design, Standard Cell Design, Data Path Cell Design.

UNIT – II: Programmable ASIC Technologies

No. of Hours: 10

Programmable ASICs and Programmable ASIC Logic Cells: The Anti fuse, Static Ram, EPROM and EEPROM Technology, Practical Issues, Specifications, PREDP Benchmarks, FPGA Economics, Actel ACT, Xilinx LCA, Altera Flex, Altera Max.

UNIT – III: ASICs and Design Software Tools

No. of Hours: 10

I/O Cells and Interconnects & Programmable ASIC Design Software: DC Output, AC Output, DC input, AC input, Clock input, Power input, Xilinx I/O block, Other I/O Cells, Actel ACT, Xilinx LCA, Xilinx EPLD, Altera Max 5000 and 7000, Altera Max 9000, Altera FLEX, Design Systems, Logic Synthesis, The Half gate ASIC.

UNIT – IV: Low-Level Design Entry and Logic Synthesis Techniques

No. of Hours: 10

Low Level Design Entry and Logic Synthesis: Schematic Entry, Low level Design Languages, PLA Tools, EDIF, a logic synthesis example, A Comparator/MUX, inside a Logic Synthesizer, Synthesis of Viterbi Decoder, Verilog and Logic synthesis, VHDL and Logic Synthesis, Finite State Machine Synthesis, Memory Synthesis, The Engine Controller, Performance Driven Synthesis, Optimization of the Viterbi decoder.

UNIT V: Simulation, Testing, and Physical Design of ASICs

No. of Hours: 10

Simulation, Test and ASIC Construction: Types of Simulation, The Comparator/MUX Example, Logic Systems, How Logic Simulation Works, Cell Models, Delay Models, Static Timing Analysis, Formal Verification, Switch Level Simulation, Transistor Level Simulation, the importance of test, Boundary Scan Test, Faults, Faults Simulation, Automatic Test Pattern Generator, Scan Test, Built in Self-Test, A simple test Example, Physical Design, CAD Tools, System Partitioning,

Textbooks:

1. Michael John Sebastian Smith, "Application Specific Integrated Circuits", Pearson Education, 2003.
2. L.J. Herbst, "Integrated Circuit Engineering", Oxford Science Publications, 1996.

Reference Books:

1. Himanshu Bhatnagar, "Advanced ASIC Chip Synthesis using Synopsis Design Compiler", 2nd Edition, Kluwer Academic, 2001.

M. Tech. VLSID
I Year - I Semester

SRET25 Regulations

L	T	P	C
0	0	4	2

(25MTVD01P) CMOS ANALOG IC DESIGN LAB
(VLSID)

Course Objectives:

- To explain the VLSI Design Methodologies using VLSI design tool.
- To grasp the significance of various CMOS analog circuits in full-custom IC Design flow
- To explain the Physical Verification in Layout Design
- To fully appreciate the design and analyze of analog and mixed signal simulation
- To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

Course Outcomes (CO):

- CO1. Analyze MOS device characteristics and extract key electrical parameters using simulation tools. (L4)
- CO2. Design and simulate basic and advanced MOS amplifier circuits, including common-source, source-degenerated, and cascode configurations, to evaluate gain and frequency response. (L3)
- CO3. Implement and analyze different current mirror topologies such as simple, cascode, and Wilson current mirrors to assess current matching and output resistance. (L4)
- CO4. Construct and evaluate differential amplifiers and operational amplifier stages to measure parameters such as CMRR, gain, stability, and compensation. (L4)
- CO5. Simulate and assess data converter circuits—including sample-and-hold, ADC, and R–2R DAC—to understand their performance metrics and conversion behavior.(L3)

List of Experiments:

The students are required to design and implement using CMOS Technology.

The students are required to implement LAYOUTS of any **SIX** Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation.

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Two stage Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

Lab Requirements:

Software: Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware: Personal Computer with necessary peripherals, configuration and operating System.

M. Tech. VLSID
I Year - I Semester

SRET25 Regulations

L	T	P	C
0	0	4	2

(25MTVD02P) CMOS DIGITAL IC DESIGN LAB
(VLSID)

Course Objectives:

- To explain the VLSI Design Methodologies using any VLSI design tool.
- To grasp the significance of various design logic Circuits in full-custom IC Design.
- To explain the Physical Verification in Layout Extraction.
- To fully appreciate the design and analyze of CMOS Digital Circuits.
- To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

Course Outcomes: On completion of the course, the student should be able to:

- CO1. Design and simulate basic combinational logic circuits such as inverters, NAND/NOR, XOR/XNOR gates, multiplexers, and full adders using digital design tools. (L3)
- CO2. Analyze the functional behavior and timing characteristics of sequential circuits including RS latches, JK flip-flops, and clock dividers. (L4)
- CO3. Design and evaluate synchronous and asynchronous counters to understand state transitions, timing, and clocking constraints. (L4)
- CO4. Implement and analyze memory elements such as static RAM cells and dynamic logic circuits to understand storage mechanisms and stability considerations. (L4)
- CO5. Develop and verify advanced digital modules such as Linear Feedback Shift Registers (LFSRs) for sequence generation and digital system applications. (L3)

List of Experiments: Any 12 experiments need to be done

The students are required to design and implement the Circuit and Layout using CMOS Technology.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software: Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

Hardware: Personal Computer with necessary peripherals, configuration and operating System.

M. Tech. VLSID
I Year - I Semester

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2	0	0	2

(25MTMB01T) RESEARCH METHODOLOGY AND IPR
(Common to SE, ES, VLSID & CSE)

Course Objectives:

- To understand the basic principles of research methodology, including research designs, types of research, ethical considerations, and proper documentation styles.
- To learn effective methods of collecting high-quality data from primary, secondary, and big data sources using appropriate tools and technologies.
- To develop skills in analyzing research data, formulating hypotheses, validating experiments, and preparing structured research reports and papers.
- To gain knowledge of the concepts, types, global frameworks, and practices of Intellectual Property Rights, including trade secrets, trademarks, and biodiversity-related IP.
- To understand the patent system, including patent application processes, examination, grant, revocation, licensing, and the role of patent agents.

Course Outcomes: On completion of the course, the student should be able to:

- CO1. Explain the fundamental concepts, types, and approaches of research, and apply ethical principles, reasoning, and documentation styles (APA/IEEE) to ensure research integrity and avoid plagiarism. (L3)
- CO2. Analyze appropriate data collection methods, sources, and technologies while ensuring data quality, reliability, and ethical handling of primary, secondary, and big data sources. (L4)
- CO3. Demonstrate skills in designing experiments, analyzing multivariate data, and developing valid hypotheses, and prepare well-structured research papers, reports, and proposals. (L6)
- CO4. Interpret the concept, evolution, and global framework of Intellectual Property Rights (IPR), and differentiate various forms such as patents, trademarks, and trade secrets in the context of WIPO, WTO, and UNESCO guidelines. (L4)
- CO5. Evaluate and apply the processes of patent filing, examination, grant, and licensing, including e-filing procedures and roles of patent agents, to protect and commercialize innovative research outcomes. (L5)

UNIT I: FUNDAMENTALS OF RESEARCH METHODOLOGY

No. of Hours: 12

Overview of research process and design - Types of Research - Approaches to Research (Qualitative vs Quantitative) - Observation studies, Experiments and Surveys - Use of Secondary and exploratory data to answer the research question - Importance of Reasoning in Research and Research ethics - Documentation Styles (APA/IEEE etc.) - Plagiarism and its consequences

UNIT II: DATA COLLECTION AND SOURCES

No. of Hours: 08

Importance of Data Collection - Types of Data - Data Collection Methods - Data Sources - primary, secondary and Big Data sources - Data Quality & Ethics - Tools and Technology for Data Collection

UNIT III: DATA ANALYSIS AND REPORTING

No. of Hours: 10

Overview of Multivariate analysis - Experimental research, cause-effect relationship, and development of hypotheses- Measurement systems analysis, error propagation, and validity of experiments - Guidelines for writing abstracts, introductions, methodologies, results, and discussions - Writing Research Papers & proposals

UNIT IV: P UNDERSTANDING INTELLECTUAL PROPERTY RIGHTS

No. of Hours: 10

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

UNIT V: PATENTS

No. of Hours: 10

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification - Types of patent application, process E-filing, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licenses, Licensing of related patents, patent agents, Registration of patent agents

Textbooks:

1. Stuart Melville and Wayne Goddard, Research Methodology: An introduction for Science & Engineering students, Juta and Company Ltd, 2004.
2. Catherine J. Holland, Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets, Entrepreneur Press, 2007.

Reference Books:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, “Business Research Methods”, Tata McGraw Hill Education 11e (2012).
2. Ranjit Kumar , Research Methodology: A Step-by-Step Guide for Beginners. . David Hunt, Long Nguyen, Matthew Rodgers, “Patent searching: tools & techniques”, Wiley, 2007.
3. Deborah E. Bouchoux , Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, 6th Edition, Cengage 2024.
4. Wayne C. Booth, Gregory G. Colomb, Joseph M. Williams, The Craft of Research, 5th Edition, University of Chicago Press, 2024
5. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, “Professional Programme Intellectual Property Rights, Law and practice”, September 2013.
6. Peter Elbow, Writing With Power, Oxford University Press, 1998.

Online Resources (Free & Authentic)

- Coursera / edX – Research Methodology and Data Analysis courses
- Springer Link & ScienceDirect – Latest journals on research design and statistics
- Google Scholar – Free access to research papers
- NCBI Bookshelf – Open-access research methodology resources
- Khan Academy (Statistics & Probability) – For fundamentals of hypothesis testing, regression, and ANOVA.

M. Tech. VLSID
I Year - I Semester

SRET25 Regulations

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**(25MTVD01S) RTL SYNTHESIS, SIMULATION AND VERIFICATION
(VLSID)**

Course Objectives:

- The simulation of combinational and sequential circuits.
- FSM based designs.
- Implementation of DFT and FFTs.
- Verify layout of basic digital circuits.

Course Outcomes: On completion of the course, the student should be able to:

- CO1. Demonstrate the process steps required for simulation /synthesis. (L2)
- CO2. Design and simulate various combinational and sequential circuits using EDA tools. (L3)
- CO3. Develop Test benches for various applications. (L3)
- CO4. Verify the simple test benches. (L4)
- CO5. Build and verify various digital circuits. (L3)

UNIT I: Introduction to RTL Design

No. of Hours: 12

RTL design flow: Specification → RTL coding → Synthesis → Simulation → Verification. HDL coding styles for synthesis (System Verilog/VHDL basics).

Lab:

1. Write synthesizable Verilog/System Verilog code for:
 - a) Half Adder, Full Adder
 - b) 4-bit Ripple Carry Adder
 - c) 4-bit Synchronous Counter (Up/Down)
2. FSM Design: Sequence Detector (e.g., detect "1011").

UNIT II: RTL Synthesis

No. of Hours:8

Synthesis concepts: mapping RTL to gate-level netlist. Constraints: clock, area, power.

Lab:

1. Synthesize combinational and sequential circuits (Adder, Counter, FSM) using EDA tool
2. Generate gate-level netlist and analyze area, delay, power reports.
3. Apply constraints (clock, timing) and observe impact on synthesis results.

UNIT III: Simulation

No. of Hours:10

Functional vs. Timing simulation. Testbench creation, waveforms, debugging.

Lab: Run simulations

1. Develop test benches for:
 - a) 4-bit ALU (add, sub, AND, OR).
 - b) Universal Shift Register.
2. Perform functional simulation using EDA tools
3. Perform post-synthesis (timing) simulation and compare results with functional simulation.

UNIT IV: Verification

No. of Hours:10

Verification basics: functional verification, assertion-based verification. Introduction to UVM/OVM concepts.

Lab: Writing simple verification test benches.

1. Write self-checking test benches for combinational and sequential circuits.
2. Use assertion-based verification (System Verilog Assertions – SVA) for protocol checks (e.g., handshaking signals).
3. Coverage-driven verification experiment: Create random test cases for FIFO/Memory.

UNIT V: Case Study & Mini Project

No. of Hours:10

Design, synthesize, and verify a digital subsystem (e.g., ALU, UART, FIFO).
End-to-end RTL → Synthesis → Simulation → Verification flow.

Lab: Design, synthesize, simulate, and verify a digital subsystem such as:

1. UART Transmitter/Receiver
2. Simple CPU Core Module (Instruction Decoder + ALU + Register File)
3. FIFO Buffer with full/empty flags

Textbooks:

1. Samir Palnitkar – Verilog HDL: A Guide to Digital Design and Synthesis.
2. Michael Ciletti – Advanced Digital Design with the Verilog HDL.
3. Chris Spear & Greg Tumbush – System Verilog for Verification.
4. David Rich – Design and Verification with System Verilog.

Reference Books:

1. Samir Palnitkar, “Verilog HDL, a guide to digital design and synthesis”, Prentice Hall 2003.
2. Doug Amos, Austin Lesea, Rene Richter, “FPGA based prototyping methodology manual”, Xilinx, 2011.
3. Bob Zeidman, “Designing with FPGAs & CPLDs”, CMP Books, 2002.

M. Tech. VLSID
I Year I Semester

SRET25 Regulations

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(25MTHS01Aa) ENGLISH FOR RESEARCH PAPER WRITING
(Common to SE, ES, VLSID & CSE)
Audit Course - I

Course Objectives:

- To equip students with the fundamentals of academic English for research paper writing.
- To develop students' advanced reading skills for analyzing and evaluating research articles.
- To refine students' grammar and language skills for clarity and precision in research writing.
- To master the skills of revising, editing, and proofreading research papers.
- To familiarize students with the role of technology and AI in research writing, including digital literacy and ethical considerations.

Course Outcomes (CO): Student will be able to

- CO1. Create well-organized academic writing outputs—titles, sub-headings, paraphrased content, and referenced paragraphs—demonstrating accuracy, cohesion, and adherence to academic writing conventions. (L6)
- CO2. Create well-organized academic notes by synthesizing information from research articles using effective note-making and summarizing techniques. (L6)
- CO3. Create well-structured and grammatically accurate academic writing sections by integrating critical reading insights and advanced grammar skills relevant to research papers. (L6)
- CO4. Create polished academic writing outputs by integrating critical and creative writing phases, applying editorial guidelines, and incorporating effective correspondence practices with journal editors(L6)
- CO5. Create ethically sound research writing by integrating fair-use principles, proper citation practices, and responsible use of AI technologies and digital tools(L6)

UNIT – I: Fundamentals of Academic English

No. of Hours: 10

Academic English - MAP (Message-Audience-Purpose) - Language Proficiency for Writing - Key Language Aspects - Clarity and Precision - Objectivity - Formal Tone - Integrating References - Word order - Sentences and Paragraphs - Link Words for Cohesion - Avoiding Redundancy / Repetition - Breaking up long sentences - Structuring Paragraphs - Paraphrasing Skills – Framing Title and Sub-headings

UNIT – II: Reading Skills for Researchers

No. of Hours: 10

Reading Academic Texts - Critical Reading Strategies - Skimming and Scanning - Primary Research Article vs. Review Article - Reading an Abstract - Analyzing Research Articles - Identifying Arguments - Classifying Methodologies - Evaluating Findings - Making Notes

UNIT – III: Grammar Refinement for Research Writing

No. of Hours: 10

Advanced Punctuation Usage - Grammar for Clarity - Complex Sentence Structures - Active- Passive Voice - Subject-Verb Agreement - Proper Use of Modifiers - Avoiding Ambiguous Pronoun References - Verb Tense Consistency - Conditional Sentences

UNIT – IV: Mastery in Refining Written Content/Editing Skills

No. of Hours: 10

Effective Revisions - Restructuring Paragraph - Editing vs Proofreading, Editing for Clarity and Coherence - Rectifying Sentence Structure Issues - Proofreading for Grammatical Precision – Spellings - Tips for Correspondence with Editors - Critical and Creative Phases of Writing

UNIT – V: Technology and Language for Research

No. of Hours: 10

Digital Literacy and Critical Evaluation of Online Content - Technology and Role of AI in Research Writing – Assistance in Generating Citations and References - Plagiarism and Ethical Considerations – Tools and Awareness – Fair Practices

Textbooks:

1. Bailey. S. Academic Writing: A Handbook for International Students. London and New York: Routledge, 2015.
2. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

Reference Books:

1. Craswell, G. Writing for Academic Success, Sage Publications, 2004.
2. Peter Elbow, Writing With Power, E-book, Oxford University Press, 2007
2. Oshima, A. & Hogue, A. Writing Academic English, Addison-Wesley, New York, 2005
3. Swales, J. & C. Feak, Academic Writing for Graduate Students: Essential Skills and Tasks. Michigan University Press, 2012.
5. Goldbort R. Writing for Science, Yale University Press (available on Google Books), 2006
6. Day R. How to Write and Publish a Scientific Paper, Cambridge University Press, 2006

Online Learning Resources:

1. <https://nptel.ac.in/noc/courses/noc20/SEM1/noc20-ge04/>
2. https://onlinecourses.swayam2.ac.in/ntr24_ed15/preview
3. "Writing in the Sciences" – Stanford University (MOOC on Coursera) <https://www.coursera.org/learn/sciwrite>
4. Academic Phrasebank – University of Manchester <http://www.phrasebank.manchester.ac.uk>
5. OWL (Online Writing Lab) – Purdue University, <https://owl.purdue.edu>
(Resources on APA/MLA formats, grammar, structure, paraphrasing)
6. Zotero or Mendeley (Reference Management Tools) – Useful for managing citations and sources.

M. Tech. VLSID
I Year I Semester

SRET25 Regulations

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(25MTSE01A) DISASTER MANAGEMENT
(Common to SE, ES, VLSID & CSE)
Audit Course - I

Course Objectives:

- Learn to demonstrate critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from Multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations
- Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

Course Outcomes: After the completion of the course, the student will be able to

- CO1. Explain the fundamental concepts of disasters, hazards, and their significance, including the classification and characteristics of natural and manmade disasters. (L2)
- CO2. Analyze the impacts of various types of disasters on human life, the economy, and the environment, and differentiate between their causes and effects. (L4)
- CO3. Apply appropriate methods and tools, such as remote sensing and meteorological data, for disaster preparedness, monitoring, and management. (L3)
- CO4. Assess disaster risk using scientific and participatory approaches, and evaluate strategies for risk reduction and survival. (L5)
- CO5. Formulate effective disaster mitigation measures by integrating structural and non-structural approaches and examine national programs and policies on disaster management. (L6)

UNIT I: Introduction:

No. of Hours: 08

Introduction:

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics.

UNIT II: Repercussions of Disasters and Hazards:

No. of Hours: 08

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanic Reactions Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT III: Disaster Preparedness and Management:

No. of Hours: 08

Preparedness: Monitoring of Phenomena Triggering A Disaster Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT IV: Risk Assessment Disaster Risk:

No. of Hours: 08

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT V: Disaster Mitigation

No. of Hours: 08

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Textbooks:

1. R.Nishith, Singh AK, "Disaster Management in India: Perspectives, issues and strategies-2020.
2. Company Sahni, Pardeep Et.Al. (Eds.), "Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi.
3. Goel S.L., Disaster Administration And Management Text And Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi.

M. Tech. VLSID
I Year I Semester

SRET25 Regulations

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(25MTHS01Ab) ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE
(Common to SE, ES, VLSID & CSE)
Audit Course - I

Course Objectives:

- To facilitate the students with the concepts of Indian traditional knowledge and to make them understand the importance of roots of knowledge system.
- To make them understand the need for protecting traditional knowledge and its significance in the global economy.
- To make them understand the legal frame work and policies related to traditional knowledge protection.
- To enable them to understand the relationship between traditional knowledge and intellectual property rights.
- To make them explore the applications of traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology

Course Outcomes: After the completion of the course, the student will be able to

- CO1. Evaluate the relevance and contemporary significance of traditional and indigenous knowledge systems in modern society (L6)
- CO2. Assess the challenges, gaps, and opportunities in the protection and commercial utilization of traditional knowledge at national and international levels (L6)
- CO3. Examine the importance of the Geographical Indications (GI) Act, 2003 in protecting region-specific traditional knowledge and supporting local economies (L6)
- CO4. Evaluate global legal forums and strategies that enhance the protection of Indian Traditional Knowledge in international platforms (L6)
- CO5. Examine the contributions of traditional knowledge to national priorities, including sustainable development, ecological balance, and cultural preservation (L6)

UNIT-I: Introduction to traditional knowledge

No. of Hours: 10

Introduction to traditional knowledge - Definition, Nature and characteristics, scope and importance - Kinds of traditional knowledge - Physical and social contexts in which traditional knowledge develop - Historical impact of social change on traditional knowledge systems - Indigenous Knowledge (IK) – Characteristics - traditional knowledge vis-à-vis indigenous knowledge -Traditional Knowledge Vs western knowledge, traditional knowledge vis-à-vis formal knowledge

UNIT-II: Protection of traditional knowledge

No. of Hours: 10

Protection of traditional knowledge- Need for protecting traditional knowledge - Significance of TK Protection - Value of TK in global economy - Role of Government to harness TK.

UNIT-III: Legal frame work and TK

No. of Hours: 10

Legal frame work and TK - A)The Scheduled Tribes and Other Traditional Forest Dwellers (Recognition of Forest Rights) Act, 2006 - Plant Varieties Protection and Farmer's Rights Act, 2001 (PPVFR Act) – B)The Biological Diversity Act 2002 and Rules 2004 - the protection of traditional knowledge bill, 2016 - Geographical Indicators Act 2003.

UNIT-IV: Traditional knowledge and Intellectual property

No. of Hours: 10

Traditional knowledge and Intellectual property - Systems of traditional knowledge protection - Legal concepts for the protection of traditional knowledge - Certain non-IPR mechanisms of traditional knowledge protection - Patents and traditional knowledge - Strategies to increase protection of traditional knowledge -Global legal FORA for increasing protection of Indian Traditional Knowledge.

UNIT-V: Traditional knowledge in different sectors

No. of Hours: 10

Traditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of

environment - Management of biodiversity, Food security of the country and protection of TK

Text Books:

1. Mahadevan, B., Bhat Vinayak Rajat, Nagendra Pavana R.N. Introduction to Indian Knowledge System: Concepts and Applications, PHI Learning Pvt.Ltd. Delhi, 2022.
2. Basanta Kumar Mohanta and Vipin Kumar Singh, Traditional Knowledge System and Technology in India, PratibhaPrakashan 2012.

Reference Books:

1. Pride of India: A Glimpse into India's Scientific Heritage, Samskrita Bharati, New Delhi.
2. Kak, S.C. "On Astronomy in Ancient India", Indian Journal of History of Science, 22(3), 1987
3. Subbarayappa, B.V. and Sarma, K.V. Indian Astronomy: A Source Book, Nehru Centre, Mumbai, 1985.
4. Bag, A.K. History of Technology in India, Vol. I, Indian National Science Academy, New Delhi, 1997.
5. Acarya, P.K. Indian Architecture, Munshiram Manoharlal Publishers, New Delhi, 1996.
6. Banerjea, P. Public Administration in Ancient India, Macmillan, London, 1961.
7. Kapoor Kapil, Singh Avadhesh, Indian Knowledge Systems Vol – I & II, Indian Institute of Advanced Study, Shimla, H.P., 2022

E-Resources:

<https://www.youtube.com/watch?v=LZP1StpYEPM> 2.<http://nptel.ac.in/courses/121106003/>