



SREE RAMA ENGINEERING COLLEGE

(AUTONOMOUS)

Approved by AICTE, New Delhi – Affiliated to JNTUA, Ananthapuramu
 Accredited by NAAC with 'A' Grade & NBA (ECE & CSE)
 Rami Reddy Nagar, Karakambadi Road, Tirupati – 517507

Department of Electronics and Communication Engineering

SRET25 - I M. Tech, I Semester Embedded Systems Course Structure

Semester-I						
S. No.	Course Code	Course Name	L	T	P	Credits
1.	25MTES01T	Microcontrollers and Programmable Digital Signal Processors	3	0	0	3
2.	25MTES02T	Advanced Digital System Design	3	0	0	3
Program Elective – I						
3.	25MTES03Ta	Advanced Microcontrollers	3	0	0	3
	25MTES03Tb	Hardware and Software Co-Design				
	25MTCS03Td	Advanced Computer Architectures				
Program Elective – II						
4.	25MTCS04Td	Advanced Computer Networks	3	0	0	3
	25MTES04Ta	SoC Architecture				
	25MTES04Tb	IOT and RTOS based Embedded System Design				
5.	25MTES01P	Digital System Design Lab	0	0	4	2
6.	25MTES02P	Microcontrollers and Programmable Digital Signal Processors Lab	0	0	4	2
7.	25MTMB01T	Research Methodology and IPR	2	0	0	2
8.	25MTES01S	IOT and RTOS for Embedded Applications	0	1	2	2
Audit Course – I						
9.	25MTHS01Aa	English for Research paper writing	2	0	0	0
	25MTSE01A	Disaster Management				
	25MTHS01Ab	Essence of Indian Traditional Knowledge				
Total			16	1	10	20

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

**(25MTES01T) MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL
PROCESSORS
(Embedded Systems)**

Course Objectives:

- To learn about ARM Microcontroller architectural features
- To understand the ARM 'C' Programming for various applications
- To study the DSP processor fundamentals and its development tools

Course Outcomes:

On completion of the course, the student should be able to:

- CO1. Understand ARM Microcontroller architectural features (L2)
- CO2. Demonstrate different types of Interrupt Controllers (L2)
- CO3. Study the on chip features of Microcontrollers (L2)
- CO4. Learn about different types of hardware modules (L2)
- CO5. Understand different families of DSP Processors. (L2)

UNIT I: ARM Cortex-Mx Processor

No. of Hours: 11

Applications, Programming model – Registers, Operation - modes, Exceptions and Interrupts, Reset Sequence, Instruction Set (ARM and Thumb), Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT II: Exception Handling and Interrupt Management in ARM Cortex-Mx

No. of Hours: 14

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT III: LPC17xx Microcontroller Architecture and On-Chip Peripherals

No. of Hours: 10

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

UNIT IV: Programmable DSP (P-DSP) Architectures and TI DSP Overview

No. of Hours: 06

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.

UNIT V: VLIW Architecture and TI TMS320C6000 Family

No. of Hours: 09

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.

Textbooks:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition.
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2nd Edition.

Reference Books:

1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.
2. Steve furber, "ARM System-on-Chip Architecture", Pearson Education
3. Frank Vahid and Tony Givargis, "Embedded System Design", Wiley
4. Technical references and user manuals on www.arm.com, NXP Semiconductor

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

(25MTES02T) ADVANCED DIGITAL SYSTEM DESIGN
(Embedded Systems)

Course Objectives:

- To understand an overview of system design approach using programmable logic devices.
- To get exposed to the various architectural features of CPLDs and FPGAs.
- To learn the methods and techniques of CPLD & FPGA design with EDA tools.
- To learn software tools used for design process with the help of case studies.

Course Outcomes:

On completion of the course, the student should be able to:

CO1. Understand an overview of system design approach using programmable logic devices. (L2)

CO2. Analyze and Design the Sequential circuits. (L4)

CO3. Design the sequential circuits with CPLD & FPGA with EDA tools. (L3)

CO4. Learn software tools used for design process with the help of case studies. (L2)

CO5. Understand fault diagnosis methods for sequential circuits. (L2)

UNIT I: Programmable Logic Devices:

No. of Hours: 10

The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, Xilinx CPLDs- Altera CPLDs, FPGAs-FPGA technology, architecture, CLB and slice Stratix LAB and ALM-RAM Blocks, Different types Xilinx FPGAs, DSP Blocks, Clock Management, I/O standards, Additional features.

UNIT II: Analysis and Derivation of Clocked Sequential Circuits with State Graphs and Tables

No. of Hours: 09

A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs-general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation.

UNIT III: Sequential Circuit Design

No. of Hours: 11

Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLDs, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design.

UNIT IV: Fault Modeling and Test Pattern Generation

No. of Hours: 15

Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model, Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults.

UNIT V: Fault Diagnosis in Sequential Circuits

No. of Hours: 05

Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Textbooks:

1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.

2. Fundamentals of Logic Design-Charles H. Roth. Jr -5th Ed. Cengage Learning.
3. Logic Design Theory-N. N. Biswas, PHI.

Reference Books:

1. Digital Circuits and Logic Design-Samuel C.LEE, PHI, 2008.
2. Digital System Design using programmable logic devices- Parag K. Lala, BS publications

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

(25MTES03Ta) ADVANCED MICROCONTROLLERS
(Embedded Systems)
Program Elective – I

Course Objectives:

- To explore the architecture and instruction set of ARM processor.
- To provide a comprehensive understanding of various programs of ARM Processors.
- To learn the programming on ARM Cortex M

Course Outcomes:

On completion of the course, the student should be able to:

- CO1. Explore the selection criteria of ARM processors by understanding the functional level trade off issues. (L4)
- CO2. Learn the ARM development towards the functional capabilities. (L2)
- CO3. Discuss ASM level program using the instruction set (L3)
- CO4. Understand the architecture of ARM Cortex M and programming on it. (L2)
- CO5. Understand the Floating Point Operations of Cortex M4 Floating Point Unit and DSP Applications. (L2)

UNIT I: ARM Embedded Systems

No. of Hours: 11

ARM Embedded Systems: RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors: Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behaviour of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence

UNIT II: Introduction to the Arm Instruction Set

No. of Hours: 11

Introduction to the Arm Instruction Set: Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set: Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT III: Technical Details of ARM Cortex M Processors

No. of Hours: 09

Technical Details of ARM Cortex M Processors: General information about Cortex-M3 and cortex M4 Processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and

system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT IV: Instruction SET of ARM Cortex M

No. of Hours: 07

Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT V: Floating Point Operations

No. of Hours: 12

Floating Point Operations: About Floating Point Data, Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU->FPCAR, FPU->FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.

Textbooks:

1. ARM System Developer's Guide Designing and Optimizing System Software by Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier Publications, 2004.
2. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu, Elsevier Publications, 3rdEdition.

Reference Books:

1. ARM System on Chip Architectures – Steve Furber, Edison Wesley, 2000.
2. ARM Architecture Reference Manual – David Seal, Edison Wesley, 2000.

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

(25MTES03Tb) HARDWARE AND SOFTWARE CO-DESIGN
(Embedded Systems)
Program Elective – I

Course Objectives:

- To acquire knowledge on various models of Co-design.
- To explore the interrelationship between Hardware and software in a embedded system.
- To acquire the knowledge of firmware development process and tools during Co-design.
- To understand validation methods and adaptability.
- To explore the system level specifications and design representation for system level synthesis.

Course Outcomes:

On completion of the course, the student should be able to:

- CO1. Acquire the knowledge on various models of Co-design. (L2)
- CO2. Explore the interrelationship between Hardware and software in an embedded system (L4)
- CO3. Acquire knowledge of the firmware development process and tools during Co-design. (L2)
- CO4. Understand validation methods and adaptability. (L2)
- CO5. Explore the system level specifications and design representation for system level synthesis.
(L4)

UNIT I: Co-Design Issues

No. of Hours: 11

Co-Design Models, Architectures, Languages, A Generic Co-design Methodology. Co-Synthesis Algorithms.

Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT II: Prototyping and Emulation

No. of Hours: 12

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT III: Compilation Techniques and Tools for Embedded Architectures

No. of Hours: 09

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT IV: Design Specification and Verification

No. of Hours: 09

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT V: Languages for System–Level Specification and Design-I

No. of Hours: 09

System–level specification, design representation for system-level synthesis, system-level specification languages.

Languages for System–Level Specification and Design-II

Heterogeneous specifications and multi-language co-simulation, the cosyma system and lycos system.

Textbooks:

1. Hardware / Software Co-Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – Springer, 2009.
2. Hardware / Software Co-Design - Giovanni De Micheli, Mariagiovanna Sami, Kluwer Academic Publishers, 2002.

Reference Books:

1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer, 2010.

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

(25MTCS03Td) ADVANCED COMPUTER ARCHITECTURES
(Embedded System)
Program Elective – I

Course Objectives:

- To impart the concepts and principles of parallel and advanced computer architectures.
- To develop the design techniques of Scalable and multithreaded Architectures.
- To apply the concepts and techniques of parallel and advanced computer architectures to design modern computer systems

Course Outcomes: After the completion of the course, student will be able to

- CO1. Analyze various parallel computer models, program partitioning techniques, and system interconnect architectures to evaluate conditions for parallelism. (L4)
- CO2. Apply performance metrics and scalability analysis to assess parallel processing applications using advanced processor and memory technologies. (L3)
- CO3. Design and differentiate linear, non-linear, instruction, and arithmetic pipelines to enhance execution performance in modern processors. (L5)
- CO4. Examine multiprocessor and multicomputer architectures, cache coherence protocols, and synchronization mechanisms for scalable system design. (L4)
- CO5. Evaluate vector and SIMD processing principles through case studies like CM-5 to identify their effectiveness in solving computationally intensive applications. (L4)

UNIT I: Fundamentals of Computer Design

No. of Hours: 12

Fundamentals of Computer design, changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT II: Pipelines and Memory Hierarchy Design

No. of Hours: 12

Pipelines:

Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design:

Introduction, review of fundamentals of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT III: Instruction Level Parallelism the Hardware Approach

No. of Hours: 10

Instruction Level Parallelism the Hardware Approach:

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach:

Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT IV: Multi Processors and Thread Level Parallelism

No. of Hours: 11

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT V: Inter Connection and Networks and Intel Architecture

No. of Hours: 10

Inter Connection and Networks:

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture: Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls.

Text Books:

1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.

Reference Books:

1. John P. Shen and Miikko H. Lipasti, Modern Processor Design: Fundamentals of Super Scalar Processors
2. Computer Architecture and Parallel Processing, Kai Hwang, Faye A.Brigs, MC Graw Hill.,
3. Advanced Computer Architecture - A Design Space Approach, DezsoSima, Terence Fountain, Peter Kacsuk, Pearson Ed.,

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

(25MTCS04Td) ADVANCED COMPUTER NETWORKS
(Embedded Systems)
Program Elective – II

Course Objectives:

- To understand various protocols in computer networks
- To learn about congestion control and quality of service in computer networks
- To study various aspects of adhoc wireless networks
- To study various aspects of wireless sensor networks

Course Outcomes (CO): After the completion of the course, student will be able to

- CO1. Understand wireless LAN concepts and standards (L2)
- CO2. Learn about congestion control and quality of service in computer networks (L2)
- CO3. Study about various aspects in Adhoc Wireless networks (L2)
- CO4. Analyze Routing protocols in Adhoc wireless networks (L4)
- CO5. Understand Wireless sensor networks concepts and Architecture(L2)

UNIT - I: Wireless LANs

No. of Hours: 10

Architectural Comparison, Characteristics, Access Control, IEEE 802.11 Project: Architecture, MAC Sub layer, Addressing Mechanism, Physical Layer, Bluetooth Architecture, Bluetooth Layers, ZigBee, WiMAX Services, IEEE Project 802.16, Cellular Telephony: operation,1G,2G,3G,4G,5G Satellite Networks, GEO, MEO and LEO Satellites

UNIT – II: Congestion Control and Quality of Service

No. of Hours: 10

Data Traffic, Congestion, Congestion Control, Quality of Service, Techniques to Improve QoS, Integrated Services, Differentiated Services, QoS in Switched Networks, Queue Management, Passive-Drop trial, Drop front, Random drop, Active- early Random drop, Random Early detection.

UNIT – III: AD HOC WIRELESS NETWORKS

No. of Hours: 12

Introduction, Cellular and Ad hoc Wireless Networks, Application of Ad Hoc Wireless Networks, Issues in Ad Hoc Wireless Networks, Medium Access Scheme, Routing, Multicasting, Transport Layer Protocols, Pricing Scheme, Quality of Service Provisioning, Self-Organization, Security, Addressing and Service Discovery, Energy Management, Scalability, Deployment Considerations, Ad Hoc Wireless Internet

UNIT – IV: Quality of Service in Ad Hoc Wireless Networks

No. of Hours: 12

Introduction, Real Time Traffic Support in Ad Hoc Wireless Networks, QoS Parameters in Ad Hoc Wireless Network, Issues and Challenges in providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions: MAC Layer Solutions, Cluster TDMA, IEEE 802.11e, DBASE, Network Layer Solutions, QoS Routing Protocols, Ticket Based QoS Routing Protocol, Predictive Location Based QoS routing protocol, Trigger Based Distributed QoS Routing Protocol, QoS enabled AODV Routing Protocol, Bandwidth QoS Routing Protocol, On Demand QoS Routing Protocol, On Demand Link-State Multipath QoS Routing Protocol, Asynchronous Slot Allocation Strategies. QoS Frameworks for Ad Hoc Wireless Networks.

UNIT – V: Wireless Sensor Networks

No. of Hours: 12

Introduction, Application of Sensor Network , Comparison with Ad hoc Wireless Networks, Issues and challenges in Designing a Sensor Network, Sensor Network Architecture, Layer Architecture, Cluster Architecture, Data Dissemination Flooding, Gossiping, Rumor Routing, Sequential Assignment Routing, Direct Diffusion, Sensor Protocols for Information via Negotiation, Cost- Field Approach, Geography Hash Table, Small Minimum Energy Communication Network, Data Gathering, Direct Transmission, Power Efficient Gathering for Sensor Information Systems, Binary Scheme, Chain Based Three-Level Scheme.

Textbooks:

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B. S. Manoj, 2004, PHI
2. Data Communications and Networking - B. A. Forouzan, 5th, 2013, TMH.

Reference Books:

1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.
2. Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

(25MTES04Ta) SOC ARCHITECTURE
(Embedded Systems)
Program Elective – II

Course Objectives:

To understand the basics related to SoC architecture and different approaches related to SoC Design, appropriate robust processor for SoC Design, appropriate memory for SoC Design and realization of real time case studies.

Course Outcomes: On completion of the course, the student should be able to:

- CO1. Demonstrate the fundamental principles of system architectures and their role in designing hardware and software system (L4)
- CO2. Evaluate and compare specialized processor architectures such as vector processors, vector instruction extensions, Very Long Instruction Word (VLIW) processors, and superscalar processors. (L4)
- CO3. Analyze simple processor-memory interactions and pipeline to optimize memory performance (L4)
- CO4. Demonstrate the practical application of bus models in designing and optimizing Interconnects and reconfigurable technologies. for embedded systems and SOCs. (L4)
- CO5. Explore advanced optimization techniques to improve the security and performance of SoC designs implementing AES and JPEG algorithms. (L4)

UNIT – I: Introduction to the System Approach

No. of Hours: 10

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory & Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II: Processors

No. of Hours: 10

Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors

UNIT – III: Memory Design for SOC

No. of Hours: 10

Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT – IV: Interconnect, Customization and Configurability

No. of Hours: 10

Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses, Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT – V: Application Studies / Case Studies**No. of Hours: 10**

SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.

Textbooks:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiley India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison Wesley Professional.

Reference Books:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.
3. System on Chip Verification – Methodologies and Techniques – Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
3	0	0	3

(25MTES04Tb) IOT AND RTOS BASED EMBEDDED SYSTEM DESIGN
(Embedded Systems)
Program Elective – II

Course Objectives:

- Understand the overview of Internet of Things, building blocks of IoT and the real-world applications.
- Analyse the IoT Physical Devices and End Points and Case studies illustrating IoT design.
- Know the importance of hard/soft Real-Time Systems and to familiarize the cases for tasks, semaphores, queues, pipes, and event flags.

Course Outcomes: On completion of the course, the student should be able to

- CO1. Understand the terminology, enabling technologies and tools of IoT. (L2)
CO2. Develop the building blocks of IoT physical devices and end points using Raspberry Pi and data analytics. (L3)
CO3. Design methodology and case study illustration of different application domains. (L5)
CO4. Analyse various scheduling algorithms and application to real time systems. (L4)
CO5. Illustrate the concepts of real time operating system and VxWorks. (L4)

UNIT I: Introduction to Internet of Things

No. of Hours: 10

Definitions & Characteristics of IoT, Physical and Logical Design of IoT, IoT Functional Blocks, IoT Communication Models, IoT Communication APIs, IOT Levels & Deployment Templates.

Tools for IoT: Chef, Chef case studies, Puppet, Puppet case study, NETCONF-YANG case studies.

UNIT II: IoT Physical Devices and End Points

No. of Hours: 09

Basic Building Blocks of an IoT Device, Raspberry Pi- about the Raspberry Pi Board, Raspberry Pi Interfaces-Serial, SPI and I2C. Introduction to Beagle Bone Black Board and its Internals.

Data Analytics For IoT: Apache Hadoop, Using Hadoop Map Reduce for Batch Data Analysis, Apache Oozie, Apache Spark, Apache Storm, using Apache Storm Real Time Data Analysis.

UNIT III: IoT Platforms Design Methodology

No. of Hours: 09

IoT Design Methodology, Case Study on IoT System for Weather Monitoring.

Case Studies illustrating IoT Design: Home Automation, Smart Parking, Weather Monitoring System, Weather Reporting Bot, Air Pollution Monitoring, Forest Fire Detection, Smart Irrigation, IoT Printer.

UNIT IV: RTOS Concepts

No. of Hours: 15

Differences between Traditional OS and RTOS, Real Time System Concepts, Hard Versus Soft Real-Time Systems: Examples, Jobs & Processors, Hard and Soft Timing Constraints, Hard Real –Time Systems, Soft Real Time Systems. Classical Uniprocessor Scheduling Algorithms –RMS, Pre-emptive EDF, Allowing for Pre-emptive and Exclusion Condition

UNIT V:

No. of Hours: 05

RTOS Kernel & Issues in Multitasking Task Assignment, Task Switching, Foreground ISRs And Background Tasks, Critical Section, Vx works – POSIX Real Time Extensions, Timeout Features, Task Creation, Semaphores (Binary, Counting), Mutex, Mailbox, Message Queues. Case Study: Automatic Vending Machine for ESD.

Textbooks:

1. Arshdeep Bahga and Vijay Madiseti, "Internet of Things - A Hands-on Approach, Universities Press", 2015.
2. Jane W.S. Liu, "Real Time Systems", Pearson Education, Asia, 2018.
3. Wind River Systems Inc., "VxWorks Programmers Guide", 2019.

Reference Books:

1. C. M. Krishna and G. Shin, "Real Time Systems", McGraw-Hill Companies Inc., 2015.

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
0	0	4	2

(25MTES01P) DIGITAL SYSTEM DESIGN LAB
(Embedded Systems)

Course Objectives: This course aims to

- To familiarize the HDL simulator / synthesis tool
- To design and implement given combinational circuit on FPGA device
- To design and implement given sequential circuit on FPGA device

Course Outcomes: On completion of the course, the student should be able to

CO1. Familiarize the HDL simulator / synthesis tool (L2)

CO2. Design and implement given combinational circuit on FPGA device (L4)

CO3. Design and implement given sequential circuit on FPGA device (L4)

List of Experiments:

Student has to design his/her user defined library components by using and standard HDL simulator / Synthesis tool for target FPGA device.

1. Combinational Logic Circuits
 - a. Generic Multiplexer.
 - b. Generic Priority Encoder.
 - c. Design of RAM Memory.
 - d. Code Converters.
 - e. Combinational Arithmetic circuits
 - f. Ripple Carry Adder.
 - g. Carry-Look ahead adder.
 - h. Signed and Unsigned Adders.
 - i. Signed and Unsigned SubStructors.
 - j. N-bit Comparator.
 - k. N – bit Arithmetic Logic Unit.
 - l. Parallel Signed and unsigned Multipliers.
 - m. Dividers.
2. Sequential Circuits
 - a. Shift Register with Load.
 - b. Switch Debouncer.
 - c. Timer.
 - d. Fibonacci Series Generator.
 - e. Frequency Meters.

Software Requirements:

Xilinx Vivado, Intel Quartus Prime Pro, Lattice Diamond, equivalent EDA software

Hardware Requirements:

Xilinx / Altera / Lattice / Equivalent FPGA development kits

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
0	0	4	2

**(25MTES02P) MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL
PROCESSORS LAB
(Embedded Systems)**

Course Objectives: This course aims to

- To write the ARM 'C' programming for applications
- To understand the interfacing of various modules with ARM 7/ ARM Cortex-M3
- To develop assembly and C Programming for DSP processors

Course Outcomes: On completion of the course, the student should be able to

- CO1. Install, configure and utilize tool sets for developing applications based on ARM processor core. (L4)
- CO2. Analyse the hardware and software interaction and integration. (L4)
- CO3. Design and develop the ARM7 based embedded systems for various applications. (L6)
- CO4. Develop application programs on ARM and DSP development boards both in assembly and C. (L6)
- CO5. Design and implement the digital filters on DSP6713 processor. (L6)

List of Experiments: Minimum 12 experiments, minimum two experiments from Part B.

Part A:

Experiments to be carried out on Cortex-Mx development boards and using GNU tool- chain

1. Blink an LED with software delay, delay generated using the Sys Tick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B:

Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

12. To develop an assembly code and C code to compute Euclidian distance between any two points
13. To develop assembly code and study the impact of parallel, serial and mixed execution
14. To develop assembly and C code for implementation of convolution operation
15. To design and implement filters in C to enhance the features of given input sequence/signal

Software Requirements:

Keil for ARM, Code Composer Studio

Hardware Requirements:

ARM Cortex Mx Development Boards, TI TMS C6713 evaluation kit.

M. Tech. ES
I Year - I Semester

SRET25 Regulations

L	T	P	C
2	0	0	2

(25MTMB01T) RESEARCH METHODOLOGY AND IPR
(Common to SE, ES, VLSID & CSE)

Course Objectives:

- To understand the basic principles of research methodology, including research designs, types of research, ethical considerations, and proper documentation styles.
- To learn effective methods of collecting high-quality data from primary, secondary, and big data sources using appropriate tools and technologies.
- To develop skills in analyzing research data, formulating hypotheses, validating experiments, and preparing structured research reports and papers.
- To gain knowledge of the concepts, types, global frameworks, and practices of Intellectual Property Rights, including trade secrets, trademarks, and biodiversity-related IP.
- To understand the patent system, including patent application processes, examination, grant, revocation, licensing, and the role of patent agents.

Course Outcomes: On completion of the course, the student should be able to:

- CO1. Explain the fundamental concepts, types, and approaches of research, and apply ethical principles, reasoning, and documentation styles (APA/IEEE) to ensure research integrity and avoid plagiarism. (L3)
- CO2. Analyze appropriate data collection methods, sources, and technologies while ensuring data quality, reliability, and ethical handling of primary, secondary, and big data sources. (L4)
- CO3. Demonstrate skills in designing experiments, analyzing multivariate data, and developing valid hypotheses, and prepare well-structured research papers, reports, and proposals. (L6)
- CO4. Interpret the concept, evolution, and global framework of Intellectual Property Rights (IPR), and differentiate various forms such as patents, trademarks, and trade secrets in the context of WIPO, WTO, and UNESCO guidelines. (L4)
- CO5. Evaluate and apply the processes of patent filing, examination, grant, and licensing, including e-filing procedures and roles of patent agents, to protect and commercialize innovative research outcomes. (L5)

UNIT I: FUNDAMENTALS OF RESEARCH METHODOLOGY

No. of Hours: 12

Overview of research process and design - Types of Research - Approaches to Research (Qualitative vs Quantitative) - Observation studies, Experiments and Surveys - Use of Secondary and exploratory data to answer the research question - Importance of Reasoning in Research and Research ethics - Documentation Styles (APA/IEEE etc.) - Plagiarism and its consequences

UNIT II: DATA COLLECTION AND SOURCES

No. of Hours: 08

Importance of Data Collection - Types of Data - Data Collection Methods - Data Sources - primary, secondary and Big Data sources - Data Quality & Ethics - Tools and Technology for Data Collection

UNIT III: DATA ANALYSIS AND REPORTING

No. of Hours: 10

Overview of Multivariate analysis - Experimental research, cause-effect relationship, and development of hypotheses- Measurement systems analysis, error propagation, and validity of experiments - Guidelines for writing abstracts, introductions, methodologies, results, and discussions - Writing Research Papers & proposals

UNIT IV: P UNDERSTANDING INTELLECTUAL PROPERTY RIGHTS

No. of Hours: 10

Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.

UNIT V: PATENTS

No. of Hours: 10

Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification - Types of patent application, process E-filing, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licenses, Licensing of related patents, patent agents, Registration of patent agents

Textbooks:

1. Stuart Melville and Wayne Goddard, Research Methodology: An introduction for Science & Engineering students, Juta and Company Ltd, 2004.
2. Catherine J. Holland, Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets, Entrepreneur Press, 2007.

Reference Books:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education 11e (2012).
2. Ranjit Kumar , Research Methodology: A Step-by-Step Guide for Beginners. . David Hunt, Long Nguyen, Matthew Rodgers, "Patent searching: tools & techniques", Wiley, 2007.
3. Deborah E. Bouchoux , Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, 6th Edition, Cengage 2024.
4. Wayne C. Booth, Gregory G. Colomb, Joseph M. Williams, The Craft of Research, 5th Edition, University of Chicago Press, 2024
5. The Institute of Company Secretaries of India, Statutory body under an Act of parliament, "Professional Programme Intellectual Property Rights, Law and practice", September 2013.
6. Peter Elbow, Writing With Power, Oxford University Press, 1998.

Online Resources (Free & Authentic)

- Coursera / edX – Research Methodology and Data Analysis courses
- Springer Link & ScienceDirect – Latest journals on research design and statistics
- Google Scholar – Free access to research papers
- NCBI Bookshelf – Open-access research methodology resources
- Khan Academy (Statistics & Probability) – For fundamentals of hypothesis testing, regression, and ANOVA.

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
0	1	2	2

(25MTES01S) IOT AND RTOS FOR EMBEDDED APPLICATIONS
(Embedded Systems)

Course Objectives: This course aims to

- Learn interfacing of sensors and actuators with IoT devices.
- Know how to integrate sensor data with cloud platforms using IoT protocols.
- Understand RTOS concepts for multitasking and task scheduling.
- Gain knowledge in inter-process communication techniques in RTOS.
- Get acquainted about IoT applications using embedded systems and RTOS

Course Outcomes: On completion of the course, the student should be able to

- CO1. Demonstrate interfacing of sensors and actuators with IoT devices. (L4)
- CO2. Acquire and integrate sensor data with cloud platforms using IoT protocols. (L3)
- CO3. Apply RTOS concepts for multitasking and task scheduling. (L3)
- CO4. Implement inter-process communication techniques in RTOS. (L3)
- CO5. Design and develop IoT applications using embedded systems and RTOS. (L5)

List of Experiments:

Module 1: IoT Hardware & Sensors:

Introduction to IoT and embedded devices, Raspberry Pi and BeagleBone Black: Architecture, GPIO, SPI, I2C interfaces, Basics of interfacing digital and analog sensors/actuators, Interfacing LEDs, Buzzer, Push Button, IR, and LDR sensors.

Experiments:

1. Setup Raspberry Pi, install OS and necessary software, test basic connectivity.
2. Interface LED and Buzzer; write Python program to blink LED periodically.
3. Interface Push Button or IR/LDR sensor; program to control LED based on input.

Module 2: IoT Data Collection & Cloud Integration:

Reading environmental sensors (temperature, humidity), IoT communication protocols: MQTT, HTTP, REST APIs, Cloud integration using Thingspeak, MQTT brokers.

Experiments:

1. Interface DHT11 sensor with Raspberry Pi; display temperature and humidity readings.
2. Upload sensor data to Thingspeak cloud and retrieve for visualization.
3. Publish and subscribe sensor data using MQTT on BeagleBone Black.

Module 3: Real-Time Operating Systems (RTOS) Fundamentals:

Differences between Traditional OS and RTOS, Hard vs. Soft real-time systems; timing constraints and task scheduling, and multitasking concepts, Scheduling algorithms.

Experiments:

1. Introduction to VxWorks RTOS: kernel, task assignment, and multitasking basics.
2. Timer programming in VxWorks.
3. Create tasks and implement Round Robin scheduling.

Module 4: Inter-Process Communication (IPC) in RTOS:

Task synchronization and communication, Semaphores: Binary and Counting, Message queues and mailboxes, Mutexes and critical sections.

Experiments:

1. Task communication using message queues in VxWorks.
2. Synchronize tasks using semaphores.
3. Implement IPC using mailboxes for data exchange between tasks.

Module 5: IoT Application Design:

Designing integrated IoT solutions combining sensors, actuators, cloud, and RTOS tasks

Experiments (Choose one):

1. Design a weather monitoring system with real-time cloud data upload.
2. Smart home automation: Control lights/fans based on sensor inputs.
3. IoT-based vending machine prototype using VxWorks and sensors.

Suggested Reading:

1. Arshdeep Bahga and Vijay Madisetti, Internet of Things: A Hands-on Approach, Universities Press, 2015.
2. Jane W.S. Liu, Real-Time Systems, Pearson Education, Asia, 2018.
3. Wind River Systems Inc., VxWorks Programmers Guide, 2019.
4. C. M. Krishna and G. Shin, Real-Time Systems, McGraw-Hill, 2015.
5. Practical Python Programming for IoT: Build advanced IoT projects using Raspberry Pi, MQTT, RESTful APIs, WebSockets, and Python 3, 2020.

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
2	0	0	0

(25MTHS01Aa) ENGLISH FOR RESEARCH PAPER WRITING
(Common to SE, ES, VLSID & CSE)
Audit Course - I

Course Objectives:

- To equip students with the fundamentals of academic English for research paper writing.
- To develop students' advanced reading skills for analyzing and evaluating research articles.
- To refine students' grammar and language skills for clarity and precision in research writing.
- To master the skills of revising, editing, and proofreading research papers.
- To familiarize students with the role of technology and AI in research writing, including digital literacy and ethical considerations.

Course Outcomes (CO): Student will be able to

- CO1. Create well-organized academic writing outputs—titles, sub-headings, paraphrased content, and referenced paragraphs—demonstrating accuracy, cohesion, and adherence to academic writing conventions. (L6)
- CO2. Create well-organized academic notes by synthesizing information from research articles using effective note-making and summarizing techniques. (L6)
- CO3. Create well-structured and grammatically accurate academic writing sections by integrating critical reading insights and advanced grammar skills relevant to research papers. (L6)
- CO4. Create polished academic writing outputs by integrating critical and creative writing phases, applying editorial guidelines, and incorporating effective correspondence practices with journal editors(L6)
- CO5. Create ethically sound research writing by integrating fair-use principles, proper citation practices, and responsible use of AI technologies and digital tools(L6)

UNIT – I: Fundamentals of Academic English

No. of Hours: 10

Academic English - MAP (Message-Audience-Purpose) - Language Proficiency for Writing - Key Language Aspects - Clarity and Precision - Objectivity - Formal Tone - Integrating References - Word order - Sentences and Paragraphs - Link Words for Cohesion - Avoiding Redundancy / Repetition - Breaking up long sentences - Structuring Paragraphs - Paraphrasing Skills – Framing Title and Sub-headings

UNIT – II: Reading Skills for Researchers

No. of Hours: 10

Reading Academic Texts - Critical Reading Strategies - Skimming and Scanning - Primary Research Article vs. Review Article - Reading an Abstract - Analyzing Research Articles - Identifying Arguments - Classifying Methodologies - Evaluating Findings - Making Notes

UNIT – III: Grammar Refinement for Research Writing

No. of Hours: 10

Advanced Punctuation Usage - Grammar for Clarity - Complex Sentence Structures - Active- Passive Voice - Subject-Verb Agreement - Proper Use of Modifiers - Avoiding Ambiguous Pronoun References - Verb Tense Consistency - Conditional Sentences

UNIT – IV: Mastery in Refining Written Content/Editing Skills

No. of Hours: 10

Effective Revisions - Restructuring Paragraph - Editing vs Proofreading, Editing for Clarity and Coherence - Rectifying Sentence Structure Issues - Proofreading for Grammatical Precision – Spellings - Tips for Correspondence with Editors - Critical and Creative Phases of Writing

UNIT – V: Technology and Language for Research

No. of Hours: 10

Digital Literacy and Critical Evaluation of Online Content - Technology and Role of AI in Research Writing – Assistance in Generating Citations and References - Plagiarism and Ethical Considerations – Tools and Awareness – Fair Practices

Textbooks:

1. Bailey. S. Academic Writing: A Handbook for International Students. London and New York: Routledge, 2015.
2. Adrian Wallwork, English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011.

Reference Books:

1. Craswell, G. Writing for Academic Success, Sage Publications, 2004.
2. Peter Elbow, Writing With Power, E-book, Oxford University Press, 2007
2. Oshima, A. & Hogue, A. Writing Academic English, Addison-Wesley, New York, 2005
3. Swales, J. & C. Feak, Academic Writing for Graduate Students: Essential Skills and Tasks. Michigan University Press, 2012.
5. Goldbort R. Writing for Science, Yale University Press (available on Google Books), 2006
6. Day R. How to Write and Publish a Scientific Paper, Cambridge University Press, 2006

Online Learning Resources:

1. <https://nptel.ac.in/noc/courses/noc20/SEM1/noc20-ge04/>
2. https://onlinecourses.swayam2.ac.in/ntr24_ed15/preview
3. "Writing in the Sciences" – Stanford University (MOOC on Coursera)
<https://www.coursera.org/learn/sciwrite>
4. Academic Phrasebank – University of Manchester
<http://www.phrasebank.manchester.ac.uk>
5. OWL (Online Writing Lab) – Purdue University, <https://owl.purdue.edu>
(Resources on APA/MLA formats, grammar, structure, paraphrasing)
6. Zotero or Mendeley (Reference Management Tools) – Useful for managing citations and sources.

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
2	0	0	0

(25MTSE01A) DISASTER MANAGEMENT
(Common to SE, ES, VLSID & CSE)
Audit Course - I

Course Objectives:

- Learn to demonstrate critical understanding of key concepts in disaster risk reduction and humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from Multiple perspectives.
- Develop an understanding of standards of humanitarian response and practical relevance in specific types of disasters and conflict situations
- Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

Course Outcomes: After the completion of the course, the student will be able to

- CO1. Explain the fundamental concepts of disasters, hazards, and their significance, including the classification and characteristics of natural and manmade disasters. (L2)
- CO2. Analyze the impacts of various types of disasters on human life, the economy, and the environment, and differentiate between their causes and effects. (L4)
- CO3. Apply appropriate methods and tools, such as remote sensing and meteorological data, for disaster preparedness, monitoring, and management. (L3)
- CO4. Assess disaster risk using scientific and participatory approaches, and evaluate strategies for risk reduction and survival. (L5)
- CO5. Formulate effective disaster mitigation measures by integrating structural and non-structural approaches and examine national programs and policies on disaster management. (L6)

UNIT I: Introduction:

No. of Hours: 08

Introduction:

Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

Disaster Prone Areas in India:

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics.

UNIT II: Repercussions of Disasters and Hazards:

No. of Hours: 08

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanic Reactions Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

UNIT III: Disaster Preparedness and Management:

No. of Hours: 08

Preparedness: Monitoring of Phenomena Triggering A Disaster Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

UNIT IV: Risk Assessment Disaster Risk:

No. of Hours: 08

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

UNIT V: Disaster Mitigation

No. of Hours: 08

Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

Textbooks:

1. R.Nishith, Singh AK, "Disaster Management in India:Perspectives,issues and strategies-2020.
2. Company Sahni, Pardeep Et.Al. (Eds.),"Disaster Mitigation Experiences and Reflections", Prentice Hall of India, New Delhi.
3. Goel S.L., Disaster Administration And Management Text And Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi.

M. Tech. ES
I Year I Semester

SRET25 Regulations

L	T	P	C
2	0	0	0

(25MTHS01Ab) ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE
(Common to SE, ES, VLSID & CSE)
Audit Course - I

Course Objectives:

- To facilitate the students with the concepts of Indian traditional knowledge and to make them understand the importance of roots of knowledge system.
- To make them understand the need for protecting traditional knowledge and its significance in the global economy.
- To make them understand the legal frame work and policies related to traditional knowledge protection.
- To enable them to understand the relationship between traditional knowledge and intellectual property rights.
- To make them explore the applications of traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology

Course Outcomes: After the completion of the course, the student will be able to

- CO1. Evaluate the relevance and contemporary significance of traditional and indigenous knowledge systems in modern society (L5)
- CO2. Assess the challenges, gaps, and opportunities in the protection and commercial utilization of traditional knowledge at national and international levels (L5)
- CO3. Examine the importance of the Geographical Indications (GI) Act, 2003 in protecting region-specific traditional knowledge and supporting local economies
- CO4. Evaluate global legal forums and strategies that enhance the protection of Indian Traditional Knowledge in international platforms (L4)
- CO5. Examine the contributions of traditional knowledge to national priorities, including sustainable development, ecological balance, and cultural preservation (L4)

UNIT-I: Introduction to traditional knowledge

No. of Hours: 10

Introduction to traditional knowledge - Definition, Nature and characteristics, scope and importance - Kinds of traditional knowledge - Physical and social contexts in which traditional knowledge develop - Historical impact of social change on traditional knowledge systems - Indigenous Knowledge (IK) – Characteristics - traditional knowledge vis-à-vis indigenous knowledge -Traditional Knowledge Vs western knowledge, traditional knowledge vis-à-vis formal knowledge

UNIT-II: Protection of traditional knowledge

No. of Hours: 10

Protection of traditional knowledge- Need for protecting traditional knowledge - Significance of TK Protection - Value of TK in global economy - Role of Government to harness TK.

UNIT-III: Legal frame work and TK

No. of Hours: 10

Legal frame work and TK - A) The Scheduled Tribes and Other Traditional Forest Dwellers (Recognition of Forest Rights) Act, 2006 - Plant Varieties Protection and Farmer's Rights Act, 2001 (PPVFR Act) – B)The Biological Diversity Act 2002 and Rules 2004 - the protection of traditional knowledge bill, 2016 - Geographical Indicators Act 2003.

UNIT-IV: Traditional knowledge and Intellectual property

No. of Hours: 10

Traditional knowledge and Intellectual property - Systems of traditional knowledge protection - Legal concepts for the protection of traditional knowledge - Certain non-IPR mechanisms of traditional knowledge protection - Patents and traditional knowledge - Strategies to increase protection of traditional knowledge -Global legal FORA for increasing protection of Indian Traditional Knowledge.

UNIT-V: Traditional knowledge in different sectors

No. of Hours: 10

Traditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of

environment - Management of biodiversity, Food security of the country and protection of TK

Text Books:

1. Mahadevan, B., Bhat Vinayak Rajat, Nagendra Pavana R.N. Introduction to Indian Knowledge System: Concepts and Applications, PHI Learning Pvt.Ltd. Delhi, 2022.
2. Basanta Kumar Mohanta and Vipin Kumar Singh, Traditional Knowledge System and Technology in India, PratibhaPrakashan 2012.

Reference Books:

1. Pride of India: A Glimpse into India's Scientific Heritage, Samskrita Bharati, New Delhi.
2. Kak, S.C. "On Astronomy in Ancient India", Indian Journal of History of Science, 22(3), 1987
3. Subbarayappa, B.V. and Sarma, K.V. Indian Astronomy: A Source Book, Nehru Centre, Mumbai, 1985.
4. Bag, A.K. History of Technology in India, Vol. I, Indian National Science Academy, New Delhi, 1997.
5. Acarya, P.K. Indian Architecture, Munshiram Manoharlal Publishers, New Delhi, 1996.
6. Banerjea, P. Public Administration in Ancient India, Macmillan, London, 1961.
7. Kapoor Kapil, Singh Avadhesh, Indian Knowledge Systems Vol – I & II, Indian Institute of Advanced Study, Shimla, H.P., 2022

E-Resources:

<https://www.youtube.com/watch?v=LZP1StpYEPM> 2.<http://nptel.ac.in/courses/121106003/>