SREE RAMA ENGINEERING COLLEGE

(AUTONOMOUS)

TIRUPATHI – 515 507 (A.P) INDIA

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Academic Regulations (SRET24) for M. Tech (Regular-Full time)

(Effective for the students admitted into I year from the Academic Year **2024-25** onwards)

SREE RAMA ENGINEERING COLLEGE
(AUTONOMOUS)

Academic Regulations of M.Tech. (Full Time/Regular) Programme

(Effective for the students admitted into I year from the Academic Year 2024-25 and onwards)

Sree Rama Engineering College (Autonomous) offers **Two** Years (**Four** Semesters) full-time Master of Technology (M.Tech.) Degree programme, under Choice Based Credit System (CBCS) in different branches of Engineering and Technology with different specializations.

The Jawaharlal Nehru Technological University Anantapur shall confer M. Tech. degree on candidates who are admitted to the programme and fulfill all the requirements for the awardof the degree.

1. Award of the M.Tech. Degree

A student will be declared eligible for the award of the M.Tech. degree if he/shefulfils the following:

1.1 Pursues a course of study for not less than two academic years and not more thanfour academic years.

1.2 Registers for 70 credits and secures all 70 credits.

2. Students, who fail to fulfil all the academic requirements for the award of the degree within four academic years from the year of their admission, shall forfeit their seat in M.Tech. course and their admission stands cancelled.

3. Programme of Study:

The following M.Tech. Specializations are offered at present in different branches of Engineering and Technology in non-autonomous affiliated colleges:

S. No.	Discipline	Name of the Specialization	Code
1	Civil Engineering	Structural Engineering	20
2	Electronics and Communication Engineering	Embedded Systems	55
		VLSI Design	57
3	Computer Science and Engineering	Computer Science & Engineering	58

and any other specializations as approved by AICTE/University from time to time.

4. Eligibility for Admissions:

4.1 Admission to the M. Tech Program shall be made subject to the eligibility, qualification and specialization prescribed by the A.P. State Government from time to time.

4.2 Admissions shall be made either on the basis of either the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by A.P. State Government (APPGECET) for M.Tech. programmes on the basis of any other exams approved by the A.P. State Government, subject to reservations as laid down by the Govt. from time to time.

5. Programme related terms:

5.1 ***Credit:*** A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (Lecture/Tutorial) or two hours of practical work/field work per week.

Credit definition:

1 Hr. Lecture (L) per week	1 credit
1 Hr. Tutorial (T) per week	1 credit
1 Hr. Practical (P) per week	0.5 credit

5.2 ***Academic Year:*** Two consecutive (one odd + one even) semesters constitute one academic year.

5.3 ***Choice Based Credit System (CBCS):*** The CBCS provides choice for studentsto select from the prescribed courses.

6. Programme Pattern:

6.1 Total duration of the M.Tech. programme is two academic years

6.2 Each academic year of study is divided into two semesters.

6.3 Each Semester shall be of 22 weeks' duration (inclusive of Examinations), witha minimum of 90 instructional days per semester.

6.4 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M.Tech. degree from the date of commencement of first year first semester, failing which the student shall

forfeit the seat in M.Tech. programme.

6.5 The medium of instruction of the programme (including examinations and project reports) will be in English only.

6.6 All subjects/courses offered for the M.Tech. degree programme are broadly classified as follows:

S. No.	Broad Course Classification	Course Category	Description
1.	Core Courses	Foundational & Professional Core Courses (PC)	Includes subjects related to the parent discipline / department / branch of Engineering
2.	Elective Courses	Professional Elective Courses (PE)	Includes elective subjects related to the parent Discipline / department / branch of Engineering
		Open Elective Courses (OE)	Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline which are of importance in the context of special skill development
3.	Research	Research Methodology & IPR	To understand importance and process of creation of patents through research
		Technical Seminar	Ensures preparedness of students to undertake major projects / Dissertation, based on core contents related to specialization
		Co-curricular Activities	Attending conferences, scientific presentations and other scholarly activities
		Dissertation	M.Tech. Project or Major Project
4.	Audit Courses	Mandatory noncredit courses	Covering subjects of developing desired attitude among the learners is on the line of initiatives such as Unnat Bharat Abhiyan, Yoga, Value education etc.

6.7 The college shall take measures to implement Virtual Labs (https://www.vlab.co.in) which provide remote access to labs in various disciplines of Engineering and will help student in learning basic and advanced concept through remote experimentation. Student shall be made to work on virtual lab experiments during the regular labs.

6.8 A faculty advisor/mentor shall be assigned to each specialization to advise students on the programme, its Course Structure and Curriculum, Choice of Courses, based on his competence, progress, pre-requisites and

interest.

6.9 Preferably 25% course work for the theory courses in every semester shall be conducted in the blended mode of learning.

7. Attendance Requirements:

7.1 A student shall be eligible to appear for the external examinations if he/she acquires i) a minimum of 50% attendance in each course and ii) 75% of attendance in aggregate of all the courses.

7.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the Academic Council.

7.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence

7.4 Students whose shortage of attendance is not condoned in any semester are noteligible to take their end examination of that class.

7.5 A stipulated fee shall be payable towards condonation of shortage of attendance.

7.6 A student will not be promoted to the next semester unless he satisfies the attendance requirements of the present semester. They may seek re-admission into that semester when offered next.

7.7 If any candidate fulfils the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

7.8 If the learning is carried out in blended mode (both offline & online), then the total attendance of the student shall be calculated considering the offline and online attendance of the student.

8. Evaluation – Distribution and Weightage of Marks:

The performance of a student in each semester shall be evaluated subject - wise (irrespective of credits assigned), for a maximum of 100 marks for theory and 100 marks for practical, based on Internal Evaluation and End Semester Examination.

8.1 There shall be five units in each of the theory subjects. For the theory subjects 60 marks will be for the End Examination and 40 marks will be for Internal Evaluation.

8.2 Two Internal Examinations shall be conducted for 30 marks each, one in the middle of the Semester and the other immediately after the completion of instruction. First mid examination shall be conducted for I & II units of the syllabus and second mid examination for III, IV & V units. Each mid exam shall be conducted for a total duration of 120 minutes with 3 questions (without choice) each question for 10 marks. Final Internal marks for a total of 30 marks shall be arrived at by considering the marks secured by the student in both the internal examinations with 80% weightage to the better internal exam and 20% to the other. There shall be an online examination (TWO) conducted during the respective mid examinations by the college for the remaining 10 marks with 20 objective questions.

8.3 The following pattern shall be followed in the End Examination:

i. Five questions shall be set from each of the five units with either/or type for 12 marks each.

ii. All the questions have to be answered compulsorily.

iii. Each question may consist of one, two or more bits.

8.4 For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day-to-day performance. The internal evaluation based on the day-to-day work-10 marks, record- 10 marks and the remaining 20 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners,with a breakup mark of Procedure-10, Experimentation-25, Results-10, Viva- voce-15.

8.5 There shall be a **Technical Seminar** during I year II semester for internal evaluation of 100 marks. A student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other faculty members of the department. The student has to secure a minimum of 50% of marks, to be declared successful. If he fails to obtain the minimum marks, he has to reappear for the same as and when supplementary

examinations are conducted. The Technical seminar shall be conducted any time during the semester as per the convenience of the Project Review Committee and students. There shall be no external examination for Technical Seminar.

8.6 There shall be Mandatory **Audit courses** in I & II semesters for zero credits. There is no external examination for audit courses. However, attendance shall be considered while calculating aggregate attendance and student shall be declared to have passed the mandatory course only when he/she secures 50% or more in the internal examinations. In case, the student fails, a re-examination shall be conducted for failed candidates for 40 marks every six months / semester satisfying the conditions mentioned in item 1 & 2 of the regulations.

8.7 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

8.8 In case the candidate does not secure the minimum academic requirement in any of the subjects he/she has to reappear for the Semester Examination either supplementary or regular in that subject or repeat the course when next offered or do any other specified subject as may be required.

8.9 The laboratory records and mid semester test papers shall be preserved for a minimum of 3 years in the respective institutions as per the College norms and shall be produced to the Committees of the University as and when the same are asked for.

9. Credit Transfer Policy

As per University Grants Commission (Credit Framework for Online Learning Courses through SWAYAM) Regulation, 2016, the college shall allow up to a maximum of 40% of the total courses being offered in a particular Programme in a semester through the Online Learning courses through SWAYAM.

9.1 The College shall offer credit mobility for MOOCs and give the equivalent credit weightage to the students for the credits earned through online

learning courses through SWAYAM platform.

9.2 The online learning courses available on the SWAYAM platform will be considered for credit transfer. SWAYAM course credits are as specified in theplatform

9.3 Student registration for the MOOCs shall be only through the institution, it is mandatory for the student to share necessary information with the institution

9.4 The institution shall select the courses to be permitted for credit transfer through SWAYAM. However, while selecting courses in the online platform institution would essentially avoid the courses offered through the curriculumin the offline mode.

9.5 The institution shall notify at the beginning of semester the list of the online learning courses eligible for credit transfer in the forthcoming Semester.

9.6 The institution shall also ensure that the student has to complete the course and produce the course completion certificate as per the academic schedule given for the regular courses in that semester

9.7 The institution shall designate a faculty member as a Mentor for each course to guide the students from registration till completion of the credit course.

9.8 The college shall ensure no overlap of SWAYAM MOOC exams with that of the external examination schedule. In case of delay in SWAYAM results, the university will re-issue the marks sheet for such students.

9.9 Student pursuing courses under MOOCs shall acquire the required credits only after successful completion of the course and submitting a certificate issued by the competent authority along with the percentage of marks and grades.

9.10 The institution shall submit the following to the examination section:

a) List of students who have passed MOOC courses in the current semester along with the certificates of completion.

b) Undertaking form filled by the students for credit transfer.

9.11 The Controller of Examination will resolve any issues that may arise in the implementation of this policy from time to time and shall review its credit

transfer policy in the light of periodic changes brought by UGC, SWAYAM, NPTEL and state government/university.

Note: Students shall be permitted to register for MOOCs offered through online platforms approved by the College/University from time to time.

10. Re-registration for Improvement of Internal Evaluation Marks:

A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and has failed in the end examination

10.1 The candidate should have completed the course work and obtained examinations results for **I, II and III** semesters.

10.2 The candidate should have passed all the subjects for which the Internal Evaluation marks secured are more than 50%.

10.3 Out of the subjects the candidate has failed in the examination due to Internal Evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of **three** Theory subjects for Improvement of Internal evaluation marks.

10.4 The candidate has to re-register for the chosen subjects and fulfill the academic requirements.

10.5 For re-registration the candidates have to apply to the COE through the Principal by paying the requisite fees and get approval from the University before the start of the semester in which re-registration is required

10.6 In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

11. Evaluation of Project/Dissertation Work:

The Project work shall be initiated at the beginning of the III Semester and the duration of the Project is of two semesters. Evaluation of Project work is for 300 marks with 200 marks for internal evaluation and 100 marks for external evaluation. Internal evaluation of the Project Work – I & Project work – II in III & IV semesters respectively shall be for 100 marks each. External evaluation of

final Project work viva voce in IV semester shall be for 100 marks.

A Project Review Committee (PRC) shall be constituted with the Head of the Department as Chairperson, Project Supervisor and one faculty member of the department offering the M.Tech. programme.

11.1 A candidate is permitted to register for the Project Work in III Semester after satisfying the attendance requirement in all the subjects, both theory and laboratory (in I & II semesters).

11.2 A candidate is permitted to submit Project dissertation with the approval ofPRC. The candidate has to pass all the theory, practical and other courses before submission of the Thesis.

11.3 Project work shall be carried out under the supervision of teacher in the parentdepartment concerned.

11.4 A candidate shall be permitted to work on the project in an industry/research organization on the recommendation of the Head of the Department. In such cases, one of the teachers from the department concerned would be the internal guide and an expert from the industry/ research organization concerned shall act as co-supervisor/ external guide. It is mandatory for the candidate to make full disclosure of all data/results on which they wish to base their dissertation. They cannot claim confidentiality simply because it would come into conflict with the Industry's or R&D laboratory's own interests. A certificate from the external supervisor is to be included in the dissertation.

11.5 Continuous assessment of Project Work - I and Project Work – II in III & IV semesters respectively will be monitored by the PRC.

11.6 The candidate shall submit status report by giving seminars in three different phases (two in III semester and one in IV semester) during the project work period. These seminar reports must be approved by the PRC before submission of the Project Thesis.

11.7 After registration, a candidate must present in Project Work Review - I, in consultation with his Project Supervisor, the title, objective and plan of action of his Project work to the PRC for approval within four weeks from the commencement of III Semester. Only after obtaining the approval of the PRC can the student initiate the project work.

11.8 The Project Work Review - II in III semester carries internal marks of 100.

Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Project Work.

11.9 A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review - II. Only after successful completion of Project Work Review – II, candidate shall be permitted for Project Work Review – III in IV Semester. The unsuccessful students in Project Work Review - II shall reappear for it as and when supplementary examinations are conducted.

11.10 The Project Work Review - III in IV semester carries 100 internal marks. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The PRC will examine the overall progress of the Project Work and decide whether or not eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review - III. If he fails to obtain the required minimum marks, he has to reappear for Project Work Review - III after a month.

11.11 For the approval of PRC the candidate shall submit the draft copy of dissertation to the Head of the Department and make an oral presentation before the PRC.

11.12 After approval from the PRC, the students are required to submit a report showing that the plagiarism is within 30%. The dissertation report will be accepted only when the plagiarism is within 30%, which shall be submitted along with the dissertation report.

11.13 Research paper related to the Project Work should be published in conference proceedings/UGC recognized journal. A copy of the published research paper should be attached to the dissertation.

11.14 After successful plagiarism check and publication of research paper, three copies of the dissertation certified by the supervisor and HOD shall be submitted to the College.

11.15 The dissertation shall be adjudicated by an external examiner selected by the Principal. For this, the HOD shall submit a panel of three examiners as submitted by the supervisor concerned for each student. However, the

dissertation will be adjudicated by one examiner nominated by the Principal.

11.16 If the report of the examiner is not satisfactory, the candidate shall revise and resubmit the dissertation, in the time frame as decided by the PRC. If report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate has to reregister for the project and complete the project within the stipulated time after taking the approval from the Academic Council.

11.17 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of Project Viva voce exam.

11.18 The Project Viva voce examinations shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who has adjudicated the dissertation. For Dissertation Evaluation (Viva voce) in IV Sem. there are external marks of 100 and it is evaluated by external examiner. The candidate has to secure a minimum of 50% marks in Viva voce exam.

11.19 If he fails to fulfill the requirements as specified, he will reappear for the Project Viva voce examination only after three months. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree.

12. Credits for Co-Curricular Activities

The credits assigned for co-curricular activities shall be given by the principal of the college and the same shall be submitted to the COE.

A Student shall earn 02 credits under the head of co-curricular activities, viz., attending Conference, Scientific Presentations and Other Scholarly Activities.
Following are the guidelines for awarding Credits for Co-Curricular Activities:

Name of the Activity	Maximum Credits / Activity
Participation in National Level Seminar / Conference / Workshop / Training programs (related to the specialization of the student)	1

Participation in International Level Seminar / Conference / workshop / Training programs held outside India (related to the specialization of the student)	2
Academic Award / Research Award from State Level / National Agencies	1
Academic Award / Research Award from International Agencies	2
Research / Review Publication in National Journals (Indexed in Scopus / Web of Science)	1
Research / Review Publication in International Journals with Editorial board outside India (Indexed in Scopus / Web of Science)	2

Note:

i) Credit shall be awarded only for the first author. Certificate of attendance and participation in a Conference/Seminar is to be submitted for awarding credit.

ii) Certificate of attendance and participation in workshops and training programs (Internal or External) is to be submitted for awarding credit. The total duration should be at least one week.

iii) Participation in any activity shall be permitted only once for acquiring required credits under co-curricular activities

13. Grading:

As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades and corresponding percentage of marks shall be followed:

After each course is evaluated for 100 marks, the marks obtained in each course will be converted to a corresponding letter grade as given below, depending on the range in which the marks obtained by the student fall.

Structure of Grading of Academic Performance

Range in which the marks in the subject fall	Grade	Grade points Assigned
≥ 90	S (Superior)	10
≥ 80 < 90	A (Excellent)	9
≥ 70 < 80	B (Very Good)	8
≥ 60 < 70	C (Good)	7
≥ 50 < 60	D (Pass)	6
< 50	F (Fail)	0
Absent	Ab (Absent)	0

i) A student obtaining Grade 'F' or Grade 'Ab' in a subject shall be considered failed and will be required to reappear for that subject when it is offered the next supplementary examination.

ii) For noncredit audit courses, "Satisfactory" or "Unsatisfactory" shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA/Percentage.

Computation of Semester Grade Point Average (SGPA) and Cumulative GradePoint Average (CGPA):

The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken bya student and the sum of the number of credits of all the courses undergone by a student, i.e.,

$$SGPA = \Sigma (C_i \times G_i)/\Sigma C_i$$

where, C_i is the number of credits of the i^{th} subject and G_i is the grade point scored by the student in the i^{th} course.

i) The Cumulative Grade Point Average (CGPA) will be computed in the same manner considering all the courses undergone by a student over all the semesters of a program, i.e.,

$$CGPA = \Sigma (C_i \times S_i)/ \Sigma C_i$$

where "S_i" is the SGPA of the i^{th} semester and C_i is the total number of credits up to that semester.

ii) Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

iii) While computing the SGPA the subjects in which the student is awarded Zero grade points will also be included.

Grade Point: It is a numerical weight allotted to each letter grade on a 10-point scale. Letter Grade: It is an index of the performance of students in a said course. Grades aredenoted by letters S, A, B, C, D and F.

14. Award of Class:

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes:

Class Awarded	Percentage of Marks to be secured
First Class with Distinction	≥70%
First Class	< 70% ≥ 60%
Pass Class	< 60% ≥ 50%

15. Exit Policy: The student shall be permitted to exit with a PG Diploma based on his/her request to the Principal through concerned head of the department at the end of first year, subject to passing all the courses in first year.

The College shall resolve any issues that may arise in the implementation of this policy from time to time and shall review the policy in the light of periodic changes brought by UGC, AICTE and State government.

16. Withholding of Results:

If the candidate has any case of in-discipline pending against him, the result of the candidate shall be withheld, and he will not be allowed/promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

17. Transitory Regulations

Discontinued, detained, or failed candidates are eligible for readmission as and when the semester is offered after fulfilment of academic regulations. Candidates who have been detained for want of attendance or not fulfilled academic requirements or who have failed after having undergone the course in earlier regulations or have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to Section 2 and they will follow the academic regulations into which they are readmitted.

18. General:

18.1 The academic regulations should be read as a whole for purpose of any interpretation.

18.2 Disciplinary action for Malpractice/improper conduct in examinations is appended.

18.3 There shall be no places transfer within the constituent colleges and affiliated colleges of Jawaharlal Nehru Technological University Anantapur.

18.4 Where the words “he”, “him”, “his”, occur in the regulations, they include “she”, “her”, “hers”.

18.5 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

18.6 The Universities may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the Universities along with recommendations of Academic Council.

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RULES FOR

DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS

	Nature of Malpractices/Improper conduct	Punishment
If the candidate:		
1.(a)	Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination)	Expulsion from the examination hall and cancellation of the performance in that subject only.
(b)	Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter.	Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him.
2.	Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester / year. The Hall Ticket of the candidate is to be cancelled.

3.	Impersonates any other candidate in connection with the examination.	The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred for four consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practical's and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for four consecutive semesters from class work and all examinations, if his involvement is established. Otherwise, the candidate is debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him.
4.	Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the

		academic regulations in connection with forfeiture of seat.
5.	Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks.	Cancellation of the performance in that subject only.
6.	Refuses to obey the orders of the Chief Superintendent / Assistant - Superintendent / any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination.	In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. If the candidate physically assaults the invigilator/ officer- in-charge of the Examinations, then the candidate is also debarred and forfeits his/her seat. In case of outsiders, they will be handed over to the police and a police case is registered against them.
7.	Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall.	Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including

		practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat.
8.	Possess any lethal weapon Or firearm in the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat.
9.	If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8.	Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person (s) who do not belong to the College will be handed over to police and, a police case will be registered against them.
10.	Comes in a drunken condition to the examination hall.	Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year.

11.	Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny.	Cancellation of the performance in that subject only or in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester / year examinations, depending on the recommendation of the committee.
12.	If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the COE or Principal for further action to award suitable punishment.	

Note:

Whenever the performance of a student is cancelled in any subject/subjects due to Malpractice, he has to register for End Examinations in that subject/subjects consequently and has to fulfil all the norms required for the award of Degree.

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SREE RAMA ENGINEERING COLLEGE

(autonomous)

Approved by AICTE, New Delhi – Affiliated to JNTUA, Ananthapuramu
Accredited by NAAC with 'A' Grade
Rami Reddy Nagar, Karakambadi road, Tirupati-517507

Department of Electronics and Communication Engineering
SRET24 I M. Tech ES - I & II Sem
Course Structure

Semester–I						
S. No.	**Course Code**	**Course Name**	**L**	**T**	**P**	**Credits**
1.	24MTES01T	Microcontrollers and Programmable Digital Signal Processors	3	0	0	3
2.	24MTES02T	Advanced Digital System Design	3	0	0	3
3.	24MTES03Ta 24MTES03Tb 24MTES03Tc	**Program Elective – I** Advanced Microcontrollers CMOS Digital IC Design Advanced Computer Architectures	3	0	0	3
4.	24MTES04Ta 24MTES04Tb 24MTES04Tc	**Program Elective – II** Embedded Real Time Operating Systems Advanced Computer Networks SoC Architecture	3	0	0	3
5.	24MTES01P	Digital System Design Lab	0	0	4	2
6.	24MTES02P	Microcontroller and Programmable DSP Lab	0	0	4	2
7.	24MTBS01T	Research Methodology and IPR	2	0	0	2
8.	24MTHS01Aa 24MTSE01A 24MTHS01Ab	**Audit Course – I** English for Research paper writing Disaster Management Sanskrit for Technical Knowledge	2	0	0	0
		Total	**16**	**0**	**8**	**18**

Semester–II						
S. No.	**Course Code**	**Course Name**	**L**	**T**	**P**	**Credits**
1.	24MTES05T	Embedded System Design	3	0	0	3
2.	24MTE206T	Embedded Programming	3	0	0	3
3.	24MTES07Ta 24MTES07Tb 24MTES07Tc	**Program Elective – III** Sensors and Actuators Modern Control Theory Artificial Intelligence and Machine Learning	3	0	0	3
4.	24MTES08Ta 24MTES08Tb 24MTES08Tc	**Program Elective – IV** Soft Computing Techniques Design of Fault Tolerant Systems Hardware and Software Co-design	3	0	0	3
5.	24MTES04P	Embedded System Design Lab	0	0	4	2
6.	24MTES05P	Embedded Programming Lab	0	0	4	2
7.	24MTES06P	Technical seminar	0	0	4	2
8.	24MTHS02La 24MTHS02Lb 24MTHS02Lc	**Audit Course – II** Pedagogy Studies Stress Management for Yoga Personality Development through Life Enlightenment Skills	2	0	0	0
		Total	**14**	**0**	**12**	**18**

Department of Electronics and Communication Engineering

SRET24 II M. Tech (ES) I & II Semester

Course Structure

M.Tech. II Year - I Semester							
S.No.	**Course codes**	**Course Name**	**Category**	**Hours per**			**Credits**
				L	T	P	
1.	24MTES09Ta 24MTES09Tb 24MTES09Tc	**Program Elective – V** Embedded Systems Protocols Communication Buses and Interfaces Robotics	PE	3	0	0	3
2.	24MTME01Ta 24MTCS02Ta 24MTME01Tb	**Open Elective** Industrial Safety Business Analytics Waste to Energy	OE	3	0	0	3
3.	24MTES01PW	Dissertation Phase – I	PR	0	0	20	10
4.	24MTES01S	Co-curricular Activities					2
		Total					**18**

M.Tech. II Year - II Semester							
S.No.	**Course codes**	**Course Name**	**Category**	**Hours per week**			**Credits**
				L	T	**P**	
1.	24MTES02PW	Dissertation Phase – II	PR	0	0	32	16
Total							**16**

L	T	P	C
3	0	0	3

(24MTES01T) Microcontrollers and Programmable Digital Signal Processors

Course Objectives:

To learn about ARM Microcontroller architectural features, to understand the ARM 'C' Programming for various applications and to study the DSP processor fundamentals and its development tools.

Course Outcomes (CO): After the completion of course, Student will be able to

CO1: Learn about ARM Microcontroller architectural features

CO2: Understand the ARM 'C' Programming for various applications

CO3: Study the DSP processor fundamentals and its development tools

UNIT – I : ARM Cortex-Mx Processor No. of Hours: 10

Applications, Programming model – Registers, Operation - modes, Exceptions and Interrupts, Reset Sequence, Instruction Set (ARM and Thumb), Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

UNIT – II : No. of Hours: 10

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency.

UNIT – III : LPC 17xx microcontroller No. of Hours: 10

- Internal memory, GPIOs, Timers, ADC, UART, I2C, CAN and other serial interfaces, PWM, RTC, WDT.

UNIT – IV : Programmable DSP (P-DSP) Processors No. of Hours: 10

Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family.

UNIT – V : TMS320C6000 Series No. of Hours: 10

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.

Text Books:

T1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition

T2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2nd Edition.

Reference Books:

R1. Sloss Andrew N, Symes Dominic, Wright Chris, “ARM System Developer's Guide: Designing and Optimizing”, Morgan Kaufman Publication.

R2. Steve furber, “ARM System-on-Chip Architecture”, Pearson Education

R3. Frank Vahid and Tony Givargis, “Embedded System Design”, Wiley

R4. Technical references and user manuals on www.arm.com, NXP Semiconductor www.nxp.com and Texas Instruments www.ti.com

L	T	P	C
3	0	0	3

(24MTES02T) Advanced Digital System Design

Course Objectives:

To understand an overview of system design approach using programmable logic devices, exposed to the various architectural features of CPLDS and FPGAS, learn the methods and techniques of CPLD & FPGA design with EDA tools and to learn software tools used for design process with the help of case studies.

Course Outcomes (CO): Student will be able to

CO1. Understand an overview of system design approach using programmable logic devices.

CO2. Get exposed to the various architectural features of CPLDS and FPGAS.

CO3. Learn the methods and techniques of CPLD & FPGA design with EDA tools.

CO4. Learn software tools used for design process with the help of case studies.

UNIT – I : Programmable Logic Devices No. of Hours: 10

The concept of programmable Logic Devices, SPLDs, PAL devices, PLA devices, GAL devices, CPLD-Architecture, Xilinx CPLDs- Altera CPLDs, FPGAs-FPGA technology, architecture, CLB and slice Stratix LAB and ALM-RAM Blocks, Different types Xilinx FPGAs, DSP Blocks, Clock Management, I/O standards, Additional features.

UNIT – II : Analysis and Derivation of Clocked Sequential Circuits No. of Hours: 10

A sequential parity checker, Analysis by signal tracing and timing charts-state tables and graphs- general models for sequential circuits, Design of a sequence detector, More Complex design problems, Guidelines for construction of state graphs, serial data conversion, Alphanumeric state graph notation.

UNIT – III : Sequential circuit Design No. of Hours: 10

Design procedure for sequential circuits-design example, Code converter, Design of Iterative circuits, Design of a comparator, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLDs, Sequential circuit design using FPGAs, Simulation and testing of Sequential circuits, Overview of computer Aided Design.

UNIT – IV : Fault Modeling and Test Pattern Generation No. of Hours: 10

Logic Fault Model, Fault detection & redundancy, Fault equivalence and fault location, Fault dominance, Single stuck at fault model, multiple Stuck at Fault models, Bridging Fault model, Fault diagnosis of combinational circuits by conventional methods, path sensitization techniques, Boolean difference method, KOHAVI algorithm, Test algorithms-D algorithm, Random testing, transition count testing, signature analysis and test bridging faults.

UNIT – V : Fault Diagnosis in Sequential Circuits No. of Hours: 10

Circuit Test Approach, Transition check Approach, State identification and fault detection experiment, Machine identification, Design of fault detection experiment.

Textbooks:

T1. Digital Electronics and design with VHDL- Volnei A. Pedroni, Elsevier publications.

T2. Fundamentals of Logic Design-Charles H.Roth,Jr. -5th Ed, ,Cengage Learning.

T3. Logic Design Theory- N.N.Biswas, PHI.

Reference Books:

R1. Digital Circuits and Logic Design-Samuel C.LEE, PHI, 2008.

L	T	P	C
3	0	0	3

(24MTES03Ta) Advanced Microcontrollers

Course Objectives:

To explore the architecture and instruction set of ARM processor, provide a comprehensive understanding of various programs of ARM Processors and to learn the programming on ARM Cortex M.

Course Outcomes (CO): Student will be able to

CO1. Explore the selection criteria of ARM processors by understanding the functional level trade off issues.

CO2. Explore the ARM development towards the functional capabilities.

CO3. Expected to work with ASM level program using the instruction set.

CO4. Understand the architecture of ARM Cortex M and programming on it.

UNIT – 1 : ARM Embedded Systems No. of Hours: 10

RISC design philosophy, ARM design philosophy, Embedded system hardware, Embedded system software.

ARM Processor Fundamentals: Registers, Current Program Status Register, Pipeline, Exceptions Interrupts and Vector Table, Core Extensions, Architecture Revisions, ARM Processor Families.

Architecture of ARM Processors Introduction to the architecture, Programmer's model- operation modes and states, registers, special registers, floating point registers, Behavior of the application program status register(APSR)-Integer status flags, Q status flag, GE bits, Memory system-Memory system features, memory map, stack memory, memory protection unit (MPU), Exceptions and Interrupts-what are exceptions?, nested vectored interrupt controller(NVIC), vector table, Fault handling, System control block (SCB), Debug, Reset and reset sequence.

UNIT – II : Introduction to the Arm Instruction Set No. of Hours: 10

Data processing instructions, branch instructions, load-store instructions, software interrupt instructions, program status register instructions, loading constants, ARMv5E extensions, Conditional execution.

Introduction to the Thumb Instruction Set

Thumb Register Usage, ARM-Thumb Interworking, Other Branch Instructions, Data Processing Instructions, Single-Register Load-Store Instructions, Multiple-Register Load-Store Instructions, Stack Instructions, Software Interrupt Instruction.

UNIT – III : Technical Details of ARM Cortex M Processors No. of Hours: 10

General information about Cortex-M3 and cortex M4 processors-Processor type, processor architecture, instruction set, block diagram, memory system, interrupt and exception support, Features of the cortex-

M3 and Cortex-M4 Processors-Performance, code density, low power, memory system, memory protection unit, interrupt handling, OS support and system level features, Cortex-M4 specific features, Ease of use, Debug support, Scalability, Compatibility.

UNIT – IV : Instruction SET of ARM Cortex M No. of Hours: 10

Background to the instruction set in ARM Cortex-M Processors, Comparison of the instruction set in ARM Cortex-M Processors, understanding the assembly language syntax, Use of a suffix in instructions, Unified assembly Language (UAL), Instruction set, Cortex-M4-specific instructions, Barrel shifter, Accessing special instructions and special registers in Programming.

UNIT – V : Floating Point Operations No. of Hours: 10

About Floating Point Data, Cortex-M4 Floating Point Unit (FPU)- overview, FP registers overview, CPACR register, Floating point register bank, FPSCR, FPU->FPCCR, FPU-> FPCAR, FPU- >FPDSCR, FPU->MVFR0, FPU->MVFR1. ARM Cortex-M4 and DSP Applications: DSP on a microcontroller, Dot Product example, writing optimized DSP code for the CortexM4-Biquad filter, Fast Fourier transform, FIR filter.

Textbooks:

T1. ARM System Developer's Guide Designing and Optimizing System Software by Andrew N. SLOSS, Dominic SYMES, Chris WRIGHT, Elsevier Publications, 2004.

T2. The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors by Joseph Yiu, Elsevier Publications, 3rdEdition.

Reference Books:

R1. ARM System on Chip Architectures – Steve Furber, Edison Wesley, 2000.

R2. ARM Architecture Reference Manual – David Seal, Edison Wesley, 2000.

L	T	P	C
3	0	0	3

(24MTVD02T) CMOS Digital IC Design
Program Elective – I

Course Objectives:

To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles, analysis of performance metrics, fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic and Combinational MOS logic circuits and Sequential MOS logic circuits, fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

Course Outcomes (CO): Student will be able to

CO1. Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,

CO2. Estimate Delay and Power of Adders circuits.

CO3. Classify different semiconductor memories.

CO4. Analyze, design and implement combinational and sequential MOS logic circuits.

CO5. Analyze complex engineering problems critically in the domain of digital IC design for conducting research.

CO6. Solve engineering problems for feasible and optimal solutions in the core area of digital ICs.

UNIT – I : MOS Design No. of Hours: 10

Pseudo NMOS Logic Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo
NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT – II : Combinational MOS Logic Circuits No. of Hours: 10

MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT – III : Sequential MOS Logic Circuits No. of Hours: 10

Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT – IV : Dynamic Logic Circuits No. of Hours: 10

Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT – V : Semiconductor Memories No. of Hours: 10

Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Textbooks :

T1. Neil Weste, David Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, 4th Edition, Pearson, 2010

T2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.

T3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.

Reference Books :

R1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

R2. Digital Integrated Circuits – A Design Perspective, Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, 2ndEdition, PHI.

M. Tech. Embedded Systems **SRET24 Regulations**
I Year M. Tech. ES – I Semester

L	T	P	C
3	0	0	3

(24MTES03Tc) Advanced Computer Architectures

Course Objectives:

To learn the instruction set architectures from a design perspective, including memory addressing, operands, and control flow, understand the advanced concepts such as instruction level parallelism, out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction, multiprocessor and parallel processing architectures and organization & design of contemporary processor architectures.

Course Outcomes (CO): Student will be able to

CO1. Learn the instruction set architectures from a design perspective, including memory addressing, operands, and control flow.

CO2. Understand the advanced concepts such as instruction level parallelism, out-of-order execution, chip-multiprocessing and the related issues of data hazards, branch costs, hardware prediction.

CO3. Study the multiprocessor and parallel processing architectures.

CO4. Learn about the organization and design of contemporary processor architectures.

UNIT – I : Fundamentals of Computer Design No. of Hours: 10

Fundamentals of Computer design, changing faces of computing and task of computer designer, Technology trends, Cost price and their trends, measuring and reporting performance, quantitative principles of computer design, Amdahl's law. Instruction set principles and examples- Introduction, classifying instruction set- memory addressing- type and size of operands, operations in the instruction set.

UNIT – II : Pipelines No. of Hours: 10

Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe line for RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.

Memory Hierarchy Design

Introduction, review of fundamentals of cache, Cache performance, Reducing cache miss penalty, Virtual memory.

UNIT – III : Instruction Level Parallelism the Hardware Approach No. of Hours: 10

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo's approach, Branch prediction, high performance instruction delivery- hardware based speculation.

ILP Software Approach

Basic compiler level techniques, static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues -Hardware verses Software.

UNIT – IV: Multi Processors and Thread Level Parallelism No. of Hours: 10

Multi Processors and Thread level Parallelism- Introduction, Characteristics of application domain, Systematic shared memory architecture, Distributed shared – memory architecture, Synchronization.

UNIT – V : Inter Connection and Networks No. of Hours: 10

Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture

Intel IA- 64 ILP in embedded and mobile markets Fallacies and pit falls.

Textbooks:

T1. John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 3rd Edition, An Imprint of Elsevier.

Reference Books:

R1. John P. Shen and Miikko H. Lipasti, Modern Processor Design : Fundamentals of Super Scalar Processors

R2. Computer Architecture and Parallel Processing ,Kai Hwang, Faye A.Brigs, MC Graw Hill.,

R3. Advanced Computer Architecture - A Design Space Approach, DezsoSima, Terence Fountain, Peter Kacsuk, Pearson Ed.,

M. Tech. Embedded Systems **SRET24 Regulations**

I Year M. Tech. ES – I Semester

L	T	P	C
3	0	0	3

(24MTES04Ta) Embedded Real Time Operating Systems

Program Elective – II

Course Objectives:

To provide broad understanding of the requirements of Real Time Operating Systems, understand, applications of these Real Time features using case studies and use the real time operating system concepts.

Course Outcomes (CO) : Student will be able to

CO1. Acquire knowledge on Real Time features of UNIX and LINUX.

CO2. Understand the basic building blocks of Real Time Operating Systems in terms of scheduling, context switching and ISR.

CO3. Understand on Real Time applications using Real Time Linux, ucos2, VX works, Embedded Linux.

UNIT – I : Introduction No. of Hours: 10

Introduction to UNIX/LINUX, Overview of Commands, File I/O, (open, create, close, seek, read, write), Process Control (fork, vfork, exit, wait, waitpid, exec).

UNIT – II : Real Time Operating Systems No. of Hours: 10

Brief History of OS, Defining RTOS, The Scheduler, Objects, Services, Characteristics of RTOS, Defining a Task, asks States and Scheduling, Task Operations, Structure, Synchronization, Communication and Concurrency.

Defining Semaphores, Operations and Use, Defining Message Queue, States, Content, Storage, Operations and Use.

UNIT – III : Objects, Services and I/O No. of Hours: 10

Pipes, Event Registers, Signals, Other Building Blocks, Component Configuration, Basic I/O Concepts, I/O Subsystem.

UNIT – IV : Exceptions, Interrupts and Timers No. of Hours: 10

Exceptions, Interrupts, Applications, Processing of Exceptions and Spurious Interrupts, Real Time Clocks, Programmable Timers, Timer Interrupt Service Routines (ISR), Soft Timers, Operations.

UNIT – V : Case Studies of RTOS No. of Hours: 10

RT Linux, Micro C/OS-II, Vx Works, Embedded Linux, and Tiny OS.

Textbooks:

T1. Real Time Concepts for Embedded Systems – Qing Li, Elsevier, 2011.

Reference Books:

R1. Embedded Systems- Architecture, Programming and Design by Rajkamal, TMH, 2007.

R2. Advanced UNIX Programming, Richard Stevens.

R3. Embedded Linux: Hardware, Software and Interfacing – Dr. Craig Hollabaugh.

M. Tech. Embedded Systems **SRET24 Regulations**

I Year M. Tech. ES – I Semester

L	T	P	C
3	0	0	3

(24MTES04Tb) Advanced Computer Networks

Program Elective – II

Course Objectives:

To understand various protocols in computer networks, congestion control and quality of service in computer networks, various aspects of adhoc wireless networks and various aspects of wireless sensor networks

Course Outcomes (CO): Student will be able to

CO1. Understand various protocols in computer networks

CO2. Learn about congestion control and quality of service in computer networks

CO3. Study various aspects of adhoc wireless networks

CO4. Study various aspects of wireless sensor networks

UNIT – I : Wireless LANs **No. of Hours: 10**

Architectural Comparison, Characteristics, Access Control, IEEE 802.11 Project: Architecture, MAC Sub layer, Addressing Mechanism, Physical Layer, Bluetooth Architecture, Bluetooth Layers, ZigBee, WiMAX Services, IEEE Project 802.16, Cellular Telephony: operation,1G,2G,3G,4G,5G
Satellite Networks, GEO, MEO and LEO Satellites

UNIT – II : Congestion Control and Quality of Service **No. of Hours: 10**

Data Traffic, Congestion, Congestion Control, Quality of Service, Techniques to Improve QoS, Integrated Services, Differentiated Services, QoS in Switched Networks,Queue Management ,Passive-Drop trial, Drop front, Random drop, Active- early Random drop, Random Early detection.

UNIT – III : AD HOC Wireless Networks **No. of Hours: 10**

Introduction, Cellular and Ad hoc Wireless Networks, Application of Ad Hoc Wireless Networks, Issues in Ad Hoc Wireless Networks, Medium Access Scheme, Routing, Multicasting, Transport Layer Protocols, Pricing Scheme, Quality of Service Provisioning, Self-Organization, Security, Addressing and Service Discovery, Energy Management, Scalability, Deployment Considerations, Ad Hoc Wireless Internet.

UNIT – IV : Quality of Service in Ad Hoc Wireless Networks **No. of Hours: 10**

Introduction, Real Time Traffic Support in Ad Hoc Wireless Networks, QoS Parameters in Ad Hoc Wireless Network, Issues and Challenges in providing QoS in Ad Hoc Wireless Networks, Classification of QoS Solutions: MAC Layer Solutions, Cluster TDMA, IEEE 802.11e, DBASE, Network Layer Solutions, QoS Routing Protocols, Ticket Based QoS Routing Protocol, Predictive Location Based QoS routing protocol, Trigger Based Distributed QoS Routing Protocol, QoS enabled AODV Routing Protocol, Bandwidth QoS Routing Protocol, On Demand QoS Routing Protocol, On Demand Link-State

Multipath QoS Routing Protocol, Asynchronous Slot Allocation Strategies. QoS Frameworks for Ad Hoc Wireless Networks.

UNIT – V : Wireless Sensor Networks **No. of Hours: 10**

Introduction, Application of Sensor Network , Comparison with Ad hoc Wireless Networks, Issues and challenges in Designing a Sensor Network, Sensor Network Architecture, Layer Architecture, Cluster Architecture, Data Dissemination Flooding, Gossiping, Rumor Routing, Sequential Assignment Routing, Direct Diffusion, Sensor Protocols for Information via Negotiation, Cost- Field Approach, Geography Hash Table, Small Minimum Energy Communication Network, Data Gathering, Direct Transmission, Power Efficient Gathering for Sensor Information Systems, Binary Scheme, Chain Based Three-Level Scheme.

Textbooks:

T1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B.S.Manoj, 2004, PHI

T2. Data Communications and Networking - B. A.Forouzan, 5th , 2013, TMH.

Reference Books:

R1. Data Communications and Computer Networks - Prakash C. Gupta, 2006, PHI.

R2. Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.

M. Tech. Embedded Systems **SRET24 Regulations**
I Year M. Tech. ES – I Semester

L	T	P	C
3	0	0	3

(24MTES04Tc) SoC Architecture

Course Objectives:

To understand the basics related to SoC architecture and different approaches related to SoC Design, appropriate robust processor for SoC Design, appropriate memory for SoC Design and realization of real time case studies.

Course Outcomes (CO): Student will be able to

CO1. Understand the basics related to SoC architecture and different approaches related to SoC Design.

CO2. Select an appropriated robust processor for SoC Design

CO3. Select an appropriate memory for SoC Design.

CO4. Realize real time case studies.

UNIT – I : Introduction to the System Approach **No. of Hours: 10**

System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory &Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

UNIT – II : Processors **No. of Hours: 10**

Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instruction extensions, VLIW Processors, Superscalar Processors

UNIT – III : Memory Design for SOC **No. of Hours: 10**

Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, Multilevel Caches, SOC Memory System, Models of Simple Processor – memory interaction.

UNIT – IV : Interconnect, Customization and Configurability **No. of Hours: 10**

Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

SOC Customization: An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT – V : Application Studies / Case Studies **No. of Hours: 10**

SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.

Textbooks:

Reference Books:

R1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer

R2. Co-Verification of Hardware and Software for ARM System on Chip Design (EmbeddedTechnology) – Jason Andrews – Newnes, BK and CDROM.

R3. System on Chip Verification – Methodologies and Techniques – Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

M. Tech. Embedded Systems **SRET24 Regulations**

I Year M. Tech. ES – I Semester

L	T	P	C
0	0	4	2

(24MTES01P) Digital System Design Lab

Course Objectives :

To Learn HDL simulator / synthesis tool, design and implemention of combinational circuit on FPGA device and sequential circuit on FPGA device.

Course Outcomes (CO) :

Familiarize the HDL simulator / synthesis tool

Design and implement given combinational circuit on FPGA device

Design and implement given sequential circuit on FPGA device

List of Experiments:

Student has to design his/her user defined library components by using and standard HDL simulator / Synthesis tool for target FPGA device.

1. Combinational Logic Circuits
    a. Generic Multiplexer.
    b. Generic Priority Encoder.
    c. Design of RAM Memory.
    d. Code Converters.
    e. Combinational Arithmetic circuits
    f. Ripple Carry Adder.
    g. Carry-Look ahead adder.
    h. Signed and Unsigned Adders.
    i. Signed and Unsigned Subtractors.
    j. N-bit Comparator.
    k. N – bit Arithmetic Logic Unit.
    l. Parallel Signed and unsigned Multipliers.
    m. Dividers.
2. Sequential Circuits
    a. Shift Register with Load.
    b. Switch Debouncer.
    c. Timer.
    d. Fibonacci Series Generator.
    e. Frequency Meters.

Software Requirements:

Xilinx Vivado, Intel Quartus Prime Pro, Lattice Diamond, equivalent EDA software.

Hardware Requirements:

Xilinx / Altera / Lattice / Equivalent FPGA development kits.

M. Tech. Embedded Systems **SRET24 Regulations**

I Year M. Tech. ES – I Semester

L	T	P	C
0	0	4	2

(24MTES02P) Microcontrollers and Programmable Digital Signal Processors Lab

Course Objectives:

To write the ARM 'C' programming for applications, interfacing of various modules with ARM 7/ ARM Cortex-M3 and assembly & C Programming for DSP processors

Course Outcomes (CO):

CO1. Install, configure and utilize tool sets for developing applications based on ARM processor core.

CO2. Design and developtheARM7 based embedded systems for various applications.

CO3. Develop application programs on ARM and DSP development boards both in assembly and C.

CO4. Design and Implement the digital filters on DSP6713 processor.

CO5. Analyze the hardware and software interaction and integration.

List of Experiments:

Part A) Experiments to be carried out on Cortex-Mx development boards and using GNU tool-chain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B) Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

12. To develop an assembly code and C code to compute Euclidian distance between any two points
13. To develop assembly code and study the impact of parallel, serial and mixed execution
14. To develop assembly and C code for implementation of convolution operation
15. To design and implement filters in C to enhance the features of given input sequence/signa

Software Requirements:

Keil for ARM, Code Composer Studio

Hardware Requirements:

ARM Cortex Mx Development Boards, TI TMS C6713 evaluation kit.

M.Tech. Embedded Systems **SRET24 Regulations**
I Year M. Tech. ES – I Semester

L	T	P	C
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(24MTBS01T) Research Methodology and IPR

Course Objectives:

Identify an appropriate research problem in their interesting domain, Preparation of a research project thesis report, law of patent and copyrights and IPR.

Course Outcomes (CO): Student will be able to

CO1. Analyze research related information

CO2. Follow research ethics

CO3. Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.

CO4. Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.

CO5. Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

UNIT – I : Introduction No. of Hours: 10

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, scope, and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

UNIT – II : Literature Study Approaches No. of Hours: 10

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, how to write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

UNIT - III : Nature of Intellectual Property No. of Hours: 10

Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

UNIT – IV : Patent Rights No. of Hours: 10

Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

UNIT – V : New Developments in IPR No. of Hours: 10

Administration of Patent System. New developments in IPR; IPR of Biological, Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

Textbooks:

T1. Stuart Melville and Wayne Goddard, “Research methodology: an introduction for science & engineering students’”

T2. Wayne Goddard and Stuart Melville, “Research Methodology: An Introduction”.

Reference Books:

R1. Ranjit Kumar, 2nd Edition, “Research Methodology: A Step by Step Guide for beginners”

R2. Halbert, “Resisting Intellectual Property”, Taylor & Francis Ltd ,2007.

R3. Mayall, “Industrial Design”, McGraw Hill, 1992.

R4. Niebel, “Product Design”, McGraw Hill, 1974.

R5. Asimov, “Introduction to Design”, Prentice Hall, 1962.

R6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, “Intellectual Property in New Technological Age”, 2016.

M. Tech. Embedded Systems **SRET24 Regulations**
I Year M. Tech. ES – II Semester

L	T	P	C
3	0	0	3

(24MTES05T) Embedded Systems Design

Course Objectives:

Differentiate between a General purpose and an Embedded System, knowledge on the building blocks of Embedded System, the requirement of Embedded firmware and its role in API.

Course Outcomes (CO): Student will be able to

CO1. Expected to differentiate the design requirements between General Purpose and Embedded Systems.

CO2. Expected to acquire the knowledge of firmware design principles.

CO3. Expected to understand the role of Real Time Operating System in Embedded Design.

CO4. To acquire the knowledge and experience of task level Communication in any Embedded System.

UNIT – I : Introduction to Embedded Systems No. of Hours: 10

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Characteristics and Quality Attributes of Embedded Systems.

UNIT – II : Typical Embedded System No. of Hours: 10

Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces. DDR , Flash, NVRAM

UNIT – III : Embedded Firmware No. of Hours: 10

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

UNIT – IV : RTOS Based Embedded System Design No. of Hours: 10

Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

UNIT - V : Task Communication No. of Hours: 10

Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

Textbooks:

T1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

Reference Books:

R1. Embedded Systems - Raj Kamal, TMH.

R2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.

R3. Embedded Systems – Lyla, Pearson, 2013

R4. An Embedded Software Primer - David E. Simon, Pearson Education.

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I Year M. Tech. ES – II Semester

L	T	P	C
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(24MTE206T) Embedded Programming

Course Objectives:

To explore the difference between general purpose programming languages and Embedded Programming Language, case studies for programming in Embedded systems.

Course Outcomes (CO): Student will be able to

CO1. Learn the basics of Embedded C with reference to 8051.

CO2. Understand how to handle control and data pins at hardware level.

CO3. Introduce objective nature of Embedded C.

CO4. Understand the specifications of real time embedded programming with case studies.

UNIT - I : PROGRAMMING EMBEDDED SYSTEMS IN C No. of Hours: 10

Introduction to embedded system, Processor used, programming language used, operating system used, developing embedded software.

INTRODUCING THE 8051 MICROCONTROLLER FAMILY: Introduction, The external interface of the Standard 8051, Reset requirements, Clock frequency and performance Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption.

UNIT – II : EMBEDDED WORLD No. of Hours: 10

Introduction Installing the Keil software and loading the project,
Configuring the simulator, Building the target, Running the simulation, Dissecting the program, Building the hardware.

UNIT – III : READING SWITCHES No. of Hours: 10

Introduction, Basic techniques for reading from port pins, Example:
Reading and writing bytes, Example: Reading and writing bits (simple version), The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code).

UNIT – IV : ADDING STRUCTURE TO YOUR CODE No. of Hours: 10

Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the ‘Hello Embedded World’ example.

MEETING REAL-TIME CONSTRAINTS: Introduction, Creating ‘hardware delays’ using Timer 0 and Timer, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, The need for ‘timeout’ mechanisms, Creating loop timeouts.

UNIT – V : CREATING AN EMBEDDED OPERATING SYSTEM No. of Hours: 10

Introduction, The basis of a simple embedded OS, Introducing sEOS, Using Timer 0 or Timer 1, alternative architectures, important design considerations when usng sEOS.

MULTI-STATE SYSTEMS AND FUNCTION SEQUENCES

Introduction, implementing a Multi-State (Timed) system, traffic light sequencing, Animatronics dinosaur, implementing a Multi- State (Input/Timed) system, Controller for a washing machine

Textbooks:

T1. Embedded C By Micheal J. Pont Pearson Education, 2002.

T2. Embedded C Coding standard-Michael Barr from Neutrino.

Reference Books:

R1. Real Time Concepts for Embedded systems-Qing Li,Caroline Yao, CMP Books 2003.

R2. Embedded/Real Time Syatems-KVKK Prasad, Dreamtech press,2005

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I Year M. Tech. ES – II Semester

L	T	P	C
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(24MTES07Ta) Sensors and Actuators

Program Elective – III

Course Objectives:

Learn about Electro mechanical sensors, use of the thermal sensors and magnetic sensors for embedded system and the basics of radiation sensors, smart sensors and actuators.

Course Outcomes (CO): Student will be able to

CO1. Learn about Electro mechanical sensors.

CO2. Learn the use of the thermal sensors and magnetic sensors for embedded system.

CO3. Learn the basics of radiation sensors, smart sensors and actuators.

UNIT – I : Sensors/Transducers No. of Hours: 10

Principles – Classification – Parameters – Characteristics - Environmental Parameters (EP) – Characterization.

Mechanical and Electromechanical Sensors: Introduction – Resistive Potentiometer – Strain Gauge – Resistance Strain Gauge – Semiconductor Strain Gauges -Inductive Sensors: Sensitivity and Linearity of the Sensor –Types-Capacitive Sensors:– Electrostatic Transducer– Force/Stress Sensors Using Quartz Resonators – Ultrasonic Sensors.

UNIT – II : Thermal Sensors No. of Hours: 10

Introduction – Gas thermometric Sensors – Thermal Expansion Type Thermometric Sensors – Acoustic Temperature Sensor – Dielectric Constant and Refractive Index thermosensors – Helium Low Temperature Thermometer – Nuclear Thermometer – Magnetic Thermometer – Resistance Change Type Thermometric Sensors –Thermoemf Sensors– Junction Semiconductor Types– Thermal Radiation Sensors –Quartz Crystal Thermoelectric Sensors – NQR Thermometry – Spectroscopic Thermometry – Noise Thermometry – Heat Flux Sensors.

Magnetic sensors: Introduction – Sensors and the Principles Behind – Magneto-resistive Sensors – Anisotropic Magnetoresistive Sensing – Semiconductor Magnetoresistors– Hall Effect and Sensors – Inductance and Eddy Current Sensors– Angular/Rotary Movement Transducers – Synchros – Synchro-resolvers - Eddy Current Sensors – Electromagnetic Flowmeter – Switching Magnetic Sensors SQUID Sensors.

UNIT – III : Radiation Sensors No. of Hours: 10

Introduction – Basic Characteristics – Types of Photosensistors/Photo detectors– X-ray and Nuclear Radiation Sensors– Fiber Optic Sensors.

Electro analytical Sensors :

Introduction – The Electrochemical Cell – The Cell Potential - Standard Hydrogen Electrode (SHE) – Liquid Junction and Other Potentials – Polarization – Concentration Polarization—Reference Electrodes - Sensor Electrodes – Electro ceramics in Gas Media.

UNIT – IV : Smart Sensors No. of Hours: 10

Introduction – Primary Sensors – Excitation – Amplification – Filters – Converters – Compensation– Information Coding/Processing - Data Communication – Standards for Smart Sensor Interface – The Automation.

Sensors –Applications

Introduction – On-board Automobile Sensors (Automotive Sensors)– Home Appliance Sensors – Aerospace Sensors — Sensors for Manufacturing –Sensors for environmental Monitoring.

UNIT – V : **Actuators** No. of Hours: 10

Pneumatic and Hydraulic Actuation Systems- Actuation systems – Pneumatic and hydraulic systems - Directional Control valves – Presure control valves – Cylinders - Servo and proportional control valves – Process control valves – Rotary actuators.

Mechanical Actuation Systems- Types of motion – Kinematic chains – Cams – Gears – Ratchet and pawl – Belt and chain drives – Bearings – Mechanical aspects of motor selection, Electrical Actuation Systems-Electrical systems -Mechanical switches – Solid-state switches Solenoids – D.C. Motors – A.C. motors – Stepper motors.

Textbooks:

T1. D. Patranabis, “Sensors and Transducers”, PHI Learning Private Limited.

T2. W. Bolton, “Mechatronics”, Pearson Education Limited.

Reference Books:

R1. Ernest O.Doebelin, Measurement Systems - Application & Design,4th Edition,Mc-GrawHill Publishing company

R2. C. Rangan , G Sarma , V.S.V. Mani Instrumentation: Devices and Systems,4th Edition,Mc- GrawHill Publishing company

M. Tech. Embedded Systems **SRET24 Regulations**
I Year M. Tech. ES – II Semester

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(24MTES07Tb) Modern Control Theory

Program Elective – III

Course Objectives:

To understand concepts of modern control system To explain the concepts of state variables analysis.
To study and analyze nonlinear control systems.
To analyze the concept of stability for nonlinear control systems and their categorization.
To apply the comprehensive knowledge of optimal theory for Control Systems.

Course Outcomes (CO): Student will be able to

Understand concepts of modern control system To explain the concepts of state variables analysis.
Study and analyze non linear control systems.
Analyze the concept of stability for nonlinear control systems and their categorization.
Apply the comprehensive knowledge of optimal theory for Control Systems.

UNIT – I : Mathematical Preliminaries and State Variable Analysis **No. of Hours: 10**

Fields, Vectors and Vector Spaces – Linear combinations and Bases – Linear Transformations and Matrices – Scalar Product and Norms – Eigen values, Eigen Vectors and a Canonical form representation of Linear systems – The concept of state – State space model of Dynamic systems – Time invariance and Linearity – Non uniqueness of state model – State diagrams for Continuous- Time State models - Existence and Uniqueness of Solutions to Continuous-Time State Equations – Solutions of Linear Time Invariant Continuous-Time State Equations – State transition matrix and it's properties. Complete solution of state space model due to zero input and due to zero state.

UNIT – II : Controllability and Observability **No. of Hours: 10**

General concept of controllability – Controllability tests, different state transformations such as diagonalization, Jordon canonical forms and Controllability canonical forms for Continuous-Time Invariant Systems – General concept of Observability – Observability tests for Continuous-Time Invariant Systems – Observability of different State transformation forms.

UNIT - III : State Feedback Controllers and Observers **No. of Hours: 10**

State feedback controller design through Pole Assignment, using Ackkermans formula– State observers: Full order and Reduced order observers.

UNIT – IV : Non-Linear Systems **No. of Hours: 10**

Introduction – Non Linear Systems - Types of Non-Linearities – Saturation – Dead-Zone - Backlash – Jump Phenomenon etc; Linearization of nonlinear systems, Singular Points and its types– Describing function–describing function of different types of nonlinear elements, – Stability analysis of Non-Linear systems through describing functions. Introduction to phase-plane analysis, Method of Isoclines for

Constructing Trajectories, Stability analysis of nonlinear systems based on phase-plane method.

UNIT – V : Stability Analysis **No. of Hours: 10**

Stability in the sense of Lyapunov, Lyapunov's stability and Lypanov's instability theorems - Stability Analysis of the Linear continuous time invariant systems by Lyapunov second method – Generation of Lyapunov functions – Variable gradient method – Krasooviski's method.

Textbooks:

T1. M.Gopal, Modern Control System Theory, New Age International - 1984

T2. Ogata. K, Modern Control Engineering, Prentice Hall - 1997

T3. N K Sinha, Control Systems, New Age International – 3rd edition.

Reference Books:

R1. Donald E.Kirk, Optimal Control Theory an Introduction, Prentice - Hall Network series - First edition.

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I Year M. Tech. ES – II Semester

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(24MTES07Tc) Artificial Intelligence and Machine Learning

Course Objectives:

To learn the difference between optimal reasoning vs human like reasoning, notions of state space representation, exhaustive search, heuristic search along with the time and space complexities, different knowledge representation techniques, applications of AI: namely Game Playing, Theorem Proving, Expert Systems, Machine Learning and Natural. Language Processing.

Course Outcomes (CO): Student will be able to

CO1. Possess the ability to formulate an efficient problem space for a problem expressed in English.

CO2. Possess the ability to select a search algorithm for a problem and characterize its time and space complexities.

CO3. Possess the skill for representing knowledge using the appropriate technique.

CO4. Possess the ability to apply AI techniques to solve problems of Game Playing, Expert Systems, Machine Learning and Natural Language Processing.

UNIT – I : Intelligent Systems No. of Hours: 10

Introduction, History, Intelligent Systems, Foundations of AI, Sub areas of AI, Applications. Problem Solving – State-Space Search and Control Strategies: Introduction, General Problem Solving, Characteristics of Problem, Exhaustive Searches, Heuristic Search Techniques, Iterative- Deepening A*, Constraint Satisfaction. Game Playing, Bounded Look-ahead Strategy and use of Evaluation Functions, Alpha-Beta Pruning

UNIT – II : Logic Concepts and Logic Programming No. of Hours: 10

Introduction, Propositional Calculus, Propositional Logic, Natural Deduction System, Axiomatic System, Semantic Tableau System in Propositional Logic, Resolution Refutation in Propositional Logic, Predicate Logic, Logic Programming. Knowledge Representation: Introduction, Approaches to Knowledge Representation, Knowledge Representation using Semantic Network, Extended Semantic Networks for KR, Knowledge Representation using Frames.

UNIT – III : Expert System and Applications No. of Hours: 10

Introduction, Phases in Building Expert Systems, Expert System Architecture, Expert Systems Vs Traditional Systems, Truth Maintenance Systems, Application of Expert Systems, List of Shells and Tools. Uncertainty Measure – Probability Theory: Introduction, Probability Theory, Bayesian Belief Networks, Certainty Factor Theory, Dempster-Shafer Theory.

UNIT – IV : Machine-Learning Paradigms No. of Hours: 10

Introduction. Machine Learning Systems. Supervised and Unsupervised Learning. Inductive Learning. Learning Decision Trees (Text Book 2), Deductive Learning. Clustering, Support Vector Machines. Artificial Neural Networks: Introduction, Artificial Neural Networks, Single- Layer Feed- Forward Networks,

Multi-Layer Feed-Forward Networks, Radial- Basis Function Networks, Design Issues of Artificial Neural Networks, Recurrent Networks.

UNIT – V : Advanced Knowledge Representation Techniques No. of Hours: 10

Case Grammars, Semantic Web Natural Language Processing: Introduction, Sentence Analysis Phases, Grammars and Parsers, Types of Parsers, Semantic Analysis, Universal Networking Knowledge.

Textbooks:

T1. Saroj Kaushik. Artificial Intelligence. Cengage Learning, 2011.

T2. Russell, Norvig: Artificial intelligence, A Modern Approach, Pearson Education, Second Edition. 2004.

Reference Books:

R1. Rich, Knight, Nair: Artificial intelligence, Tata McGraw Hill, Third Edition 2009.

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I Year M. Tech. ES – II Semester

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(24MTES08Ta) Soft Computing Techniques

Program Elective – IV

Course Objectives:

To understand the concepts of different types neural networks, fuzzy logic systems and concepts of genetic algorithm

Course Outcomes (CO): Student will be able to

CO1. Understand the concepts of different types neural networks

CO2. Understand the concepts of fuzzy logic systems

CO3. Learn concepts of genetic algorithm

UNIT – I : Fundamentals of Neural Networks & Feed Forward Networks No. of Hours: 10

Basic Concept of Neural Networks, Human Brain, Models of an Artificial Neuron, Learning Methods, Neural Networks Architectures.

Feed Forward Neural Network: Single Layer Feed Forward Neural Network, The Perceptron Model, Multilayer Feed Forward Neural Network, Architecture of a Back Propagation Network(BPN), The Solution, Backpropagation Learning, Selection of various Parameters in BPN. Application of Back propagation Networks in Pattern Recognition & Image Processing.

UNIT – II : Associative Memories & ART Neural Networks No. of Hours: 10

Basic concepts of Linear Associator, Basic concepts of Dynamical systems, Mathematical Foundation of Discrete-Time Hop field Networks(HPF), Mathematical Foundation of Gradient-Type Hopfield Networks, Transient response of Continuous Time Networks, Applications of HPF in Solution of Optimization Problem: Minimization of the Traveling salesman tour length, Summing networks with digital outputs, Solving Simultaneous Linear Equations, Bidirectional Associative Memory Networks; Cluster Structure, Vector Quantization, Classical ART Networks, Simplified ART Architecture

UNIT – III: Fuzzy Logic & Systems: No. of Hours: 10

Fuzzy sets, Crisp Relations, Fuzzy Relations, Crisp Logic, Predicate Logic, Fuzzy Logic, Fuzzy Rule based system, Defuzzification Methods, Applications: Greg Viot's, zzy Cruise Controller, Air Conditioner Controller.

UNIT - IV : Genetic Algorithms No. of Hours: 10

Basic Concepts of Genetic Algorithms (GA), Biological background, Creation of Offsprings, Working Principle, Encoding, Fitness Function, Reproduction, Inheritance Operators, Cross Over, Inversion and Deletion, Mutation Operator, Bit-wise Operators used in GA, Generational Cycle, Convergence of

Genetic Algorithm.

UNIT – V : Hybrid Systems No. of Hours: 10

Types of Hybrid Systems, Neural Networks, Fuzzy Logic, and Genetic Algorithms Hybrid, Genetic Algorithm based BPN: GA Based weight Determination, Fuzzy Back Propagation Networks: LR-type fuzzy numbers, Fuzzy Neuron, Fuzzy BP Architecture, Learning in Fuzzy BPN, Inference by fuzzy BPN.

Textbooks:

T1. Introduction to Artificial Neural Systems - J.M.Zurada, Jaico Publishers

T2. Neural Networks, Fuzzy Logic & Genetic Algorithms: Synthesis & Applications - S.Rajasekaran, G.A. VijayalakshmiPai, July 2011, PHI, New Delhi.

T3. Genetic Algorithms by David E. Gold Berg, Pearson Education India, 2006.

T4. Neural Networks & Fuzzy Sytems- Kosko.B., PHI, Delhi,1994.

Reference Books:

R1. Artificial Neural Networks - Dr. B. Yagananarayana, 1999, PHI, New Delhi.

R2. An introduction to Genetic Algorithms - Mitchell Melanie, MIT Press, 1998

R3. Fuzzy Sets, Uncertainty and Information- Klir G.J. & Folger. T. A., PHI, Delhi, 1993.

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I Year M. Tech. ES – II Semester

L	T	P	C
3	0	0	3

(24MTES08Tb) Design of Fault Tolerant Systems

Program Elective – IV

Course Objectives:

Broad understanding of fault diagnosis and tolerant design approach, framework of test pattern generation using semi and full automatic approach, scan architectures and acquire the knowledge of design of built-in-self test.

Course Outcomes (CO): Student will be able to

CO1. Provide broad understanding of fault diagnosis and tolerant design approach.

CO2. Illustrate the framework of test pattern generation using semi and full automatic approach.

CO3. Acquire the knowledge of scan architectures.

CO4. Acquire the knowledge of design of built-in-self test.

UNIT – I : Fault Tolerant Design **No. of Hours: 10**

Basic concepts: Reliability concepts, Failures & faults, Reliability and Failure rate, Relation between reliability and mean time between failure, maintainability and availability, reliability of series, parallel and parallel-series combinational circuits.

Fault Tolerant Design : Basic concepts-static, dynamic, hybrid, triple modular redundant system (TMR), 5MR reconfiguration techniques, Data redundancy, Time redundancy and software Redundancy concepts.

UNIT – II : Self Checking circuits & Fail safe Design **No. of Hours: 10**

Basic concepts of self checking circuits, Design of Totally self checking checker, Checkers using m out of n codes, Berger code, Low cost residue code, Fail Safe Design- Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self checking PLA design.

UNIT – III : Design for Testability **No. of Hours: 10**

Design for testability for combinational circuits: Basic concepts of Testability, Controllability and observability, The Reed Muller's expansion technique, use of control and syndrome testable designs. Design for testability by means of scan Making circuits Testable, Testability Insertion, Full scan DFT technique- Full scan insertion, flip- flop Structures, Full scan design and Test, Scan Architectures-full scan design, Shadow register DFT, Partial scan methods, multiple scan design, other scan designs.

UNIT – IV : Logic Built-in-self-test **No. of Hours: 10**

BIST Basics-Memory-based BIST,BIST effectiveness, BIST types, Designing a BIST, Test Pattern Generation-Engaging TPGs, exhaustive counters, ring counters, twisted ring counter, Linear feedback shift register, Output Response Analysis-Engaging ORA's, One's counter, transition counter, parity checking, Serial LFSRs, Parallel Signature analysis, BIST architectures-BIST related terminologies, A centralised and separate Board-level BIST architecture, Built-in evaluation and self test(BEST), Random Test socket(RTS), LSSD On-chip self test, Self –testing using MISR and SRSG, Concurrent BIST, BILBO, Enhancing coverage, RT level BIST design-CUT design, simulation and synthesis, RTS BIST insertion, Configuring the RTS BIST, incorporating configurations in BIST, Design of STUMPS, RTS and STUMPS results.

UNIT – V : Standard IEEE Test Access Methods **No. of Hours: 10**

Boundary Scan Basics, Boundary scan architecture- Test access port, Boundary scan registers, TAP controller, the decoder unit, select and other units, Boundary scan Test Instructions-Mandatory instructions, Board level scan chain structure-One serial scan chain, multiple-scan chain with one control test port, multiple-scan chains with one TDI,TDO but multiple TMS, Multiple-scan chain, multiple access port, RT Level boundary scan-inserting boundary scan test hardware for CUT, Two module test case, virtual boundary scan tester, Boundary Scan Description language.

Textbooks:

T1. Fault Tolerant & Fault Testable Hardware Design- Parag K.Lala,PHI, 1984.

T2. Digital System Test and Testable Design using HDL models and Architectures - ZainalabedinNavabi, Springer International Ed.,

Reference Books:

R1. Digital Systems Testing and Testable Design-MironAbramovici, Melvin A.Breuer and Arthur D. Friedman, Jaico Books

R2. Essentials of Electronic Testing- Bushnell &VishwaniD.Agarwal,Springers.

R3. Design for Test for Digital IC's and Embedded Core Systems- Alfred L. Crouch, 2008

M. Tech. Embedded Systems **SRET24 Regulations**
I Year M. Tech. ES – II Semester

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(24MTES08Tc) Hardware and Software Co-Design

Program Elective – IV

Course Objectives:

To acquire the knowledge on various models of Co-design, interrelationship between Hardware and software in a embedded system, firmware development process and tools during Co-design and validation methods and adaptability.

Course Outcomes (CO): Student will be able to

CO1. Acquire the knowledge on various models of Co-design.

CO2. Explore the interrelationship between Hardware and software in a embedded system

CO3. Acquire the knowledge of firmware development process and tools during Co-design.

CO4. Understand validation methods and adaptability.

UNIT – I : Co- Design Issues **No. of Hours: 10**

Co- Design Models, Architectures, Languages, A Generic Co-design Methodology. Co- Synthesis Algorithms Hardware software synthesis algorithms: hardware – software partitioning distributed system co- synthesis.

UNIT – II : Prototyping and Emulation **No. of Hours: 10**

Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques, system communication infrastructure.

Target Architectures

Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT – III : Compilation Techniques for Embedded Processor Architectures **No. of Hours: 10**

Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration in a compiler development environment.

UNIT – IV : Design Specification and Verification **No. of Hours: 10**

Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT – V : Languages for System – Level Specification and Design-I **No. of Hours: 10**

System – level specification, design representation for system level synthesis, system level specification languages,

Languages for System – Level Specification and Design-II

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

Textbooks:

T1. Hardware / Software Co- Design Principles and Practice – Jorgen Staunstrup, Wayne Wolf – Springer, 2009.

T2. Hardware / Software Co- Design - Giovanni De Micheli, Mariagiovanna Sami,Kluwer Academic Publishers, 2002.

Reference Books:

R1. A Practical Introduction to Hardware/Software Co-design -Patrick R. Schaumont, Springer, 2010.

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I Year M. Tech. ES – II Semester

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(24MTES04P) Embedded System Design Lab

Course Objectives:

To familiarize with embedded systems programming concepts

To implement different embedded communication and interfacing protocols

Course Outcomes (CO):

Familiarize with embedded systems programming concepts

Implement different embedded communication and interfacing protocols

List of Experiments:

1. Functional Testing of Devices: Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. Exporting Display on to other Systems: Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. GPIO Programming: Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. Interfacing Chronos eZ430: Chronos device is a programmable Texas Instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacing with devices.
5. ON/OFF Control Based On Light Intensity: Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF the high intensity LED's by taking some pre-defined threshold light intensity value.
6. Battery Voltage Range Indicator: Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 LEDs, turn on 3 LED s for 2-3V, 2 LEDs for 1-2V, 1 LED for 0.1-1V & turn off all for 0V)
7. Dice Game Simulation: Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. Displaying RSS News Feed On Display Interface: Displaying the RSS news feed headlines on a LCD display connected to device. This can be adapted to other websites like twitter or other information websites. Python can be used to acquire data from the internet.
9. Porting Open w.r.t the Device: Attempt to use the device while connecting to a WiFi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. Hosting a website on Board: Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and thereby host the website.
11. Webcam Server: Interfacing the regular USB webcam with the device and turn it into fully functional IP webcam & test the functionality.
12. FM Transmission: Transforming the device into a regular FM transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

Software Requirements: Keil / Python

Hardware Requirements: Arduino/Raspbery Pi/Beaglebone

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(24MTES05P) Embedded Programming Lab

Course Objectives:

To understand the concepts of Embedded 'C' programming

To implement given program on 8051 microcontrollers

To implement given program on LPC2148 microcontroller

Course Outcomes (CO):

Understand the concepts of Embedded 'C' programming

Implement given program on 8051 microcontrollers

Implement given program on LPC2148 microcontroller

List of Experiments:

Embedded C programming and testing using 8051 advanced development board and KEIL tools.

1. (i) Program to perform arithmetic operations.
   (ii) Program to perform sorting of numbers.
2. Program to shift LED's Left and right.
3. Program for DIP switch interface.
4. Program to display message in LCD 8 bit mode.
5. Program to display picture in GLCD 128X64.
6. Program to send data serially through serial port.
7. Program to display I2C RTC(DS1307) to Hyper terminal window.
8. Program to display digital temperature sensor output.
9. Program for 4X4 matrix keyboard with LCD.
10. Program to interface stepper motor.
11. Program to interface relay.

Embedded C programming and testing using LPC2148 development kit(Real time environment)

1. Program to interface LED and implement Multi-tasking.
2. Program to display RTC-ADC on LCD.
3. Program to display message on GLCD

Software Requirements: Keil for C51, Keil for ARM

Hardware Requirements: 8051 Development boards, LPC2148 Development boards

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(24MTES09Ta) EMBEDDED SYSTEMS PROTOCOLS

(ES)

Course Objectives:

- To acquire knowledge on communication protocols of connecting Embedded Systems.
- To understand the design parameters of USB and CAN bus protocols.
- To understand the design issues of Ethernet in Embedded networks.
- To acquire the knowledge of wireless protocols in Embedded domain.

Course Outcomes:

After completion of the course, the student should be able to:

CO1. Demonstrate knowledge on communication protocols of connecting Embedded Systems (L2)

CO2. Understand the design parameters of USB and CAN bus protocols (L2)

CO3. Analyze the design issues of Ethernet in Embedded networks (L4)

CO4. Design different Ethernet controllers (L6)

CO5. Describe the knowledge of wireless protocols in Embedded domain (L2)

UNIT I: Embedded Communication Protocols: **No. of Hours: 08**

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols - RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming - ISA/PCI Bus protocols –Firewire.

UNIT II: USB and CAN Bus: **No. of Hours: 11**

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication Packets –Data flow types –Enumeration –Descriptors –PIC 18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing –PIC microcontroller CAN Interface –A simple application with CAN.

UNIT III: Ethernet Basics: **No. of Hours: 10**

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications – Inside the Internet protocol, VLAN, Network Redundancy.

UNIT IV: Embedded Ethernet: **No. of Hours: 08**

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Email for Embedded Systems – Using FTP – Keeping Devices and Network secure, ICMP and IGMP protocols.

UNIT V: Wireless Embedded Networking: **No. of Hours: 08**

Wireless sensor networks – Introduction – Applications – Network Topology – Localization –Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing –Data Centric routing.

Textbooks:

1. Embedded Systems Design: A Unified Hardware/Software Introduction - Frank Vahid, Tony Givargis, John & Wiley Publications, 2002.
2. Parallel Port Complete: Programming, interfacing and using the PCs parallel printer port - Jan Axelson, Penram Publications, 1996.

Reference Books:

1. Advanced PIC microcontroller projects in C: from USB to RTOS with the PIC18F series - Dogan Ibrahim, Elsevier 2008.
2. Embedded Ethernet and Internet Complete - Jan Axelson, Penram publications, 2003.
3. Networking Wireless Sensors – Bhaskar Krishnamachari, Cambridge press 2005.

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(24MTES09Tb) COMMUNICATION BUSES AND INTERFACES

(ES)

Course Objectives:

- To understand the concepts of different types of serial buses.
- To learn about CAN, PCIe and USB architecture
- To learn about data streaming using serial communication protocols

Course Outcomes:

After completion of the course, the student should be able to:

CO1. Understand the concepts of different types of serial buses(L2)

CO2. Learn about CAN, PCIe and USB architecture (L2)

CO3. Describe about data streaming using serial communication protocols (L2)

CO4. Illustrate about different types of transfer types and descriptive types in USB (L2)

CO5. Learn about data streaming using serial communication protocols (L2)

UNIT I: Serial Busses **No. of Hours: 08**

Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features, Limitations and applications of RS232, RS485, I2C, SPI, and PCI Express.

UNIT II: CAN Architecture **No. of Hours: 10**

ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

UNIT III: PCIe **No. of Hours: 08**

Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

UNIT IV: USB **No. of Hours: 10**

Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration- Device detection, Default state, Addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver

UNIT V: Data streaming Serial Communication Protocol: **No. of Hours: 08**

Serial Front Panel Data Port(SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable, and UART.

Textbooks:

1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.
2. Serial Port Complete-COM Ports, USB Virtual Com Portsand Ports for Embedded Systems- Jan Axelson, Lakeview Research, 2nd Ed.,

Reference Books:

1. USB Complete – Jan Axelson, Penram Publications.
2. PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.

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(24MTES09Tc) ROBOTICS

(ES)

Course Objectives:

- To describe the various elements that make an industrial robot system
- To discuss various applications of industrial robot systems
- To analyze robot manipulators in terms of their kinematics, kinetics, and control
- To design a model robot manipulators and analyze their performance, through running simulations using a MATLAB-based Robot Toolbox

Course Outcomes:

After completion of the course, the student should be able to:

CO1. Describe the various elements that make an industrial robot system (L2)

CO2. Analyze robot manipulators in terms of their kinematics, kinetics, and control (L4)

CO3. Analyze static and dynamic modeling (L4)

CO4. Design a model robot manipulators and analyze their performance, through running simulations using a MATLAB-based Robot Toolbox (L6)

CO5. Discuss various applications of industrial robots and non-industrial robots. (L2)

UNIT I: Introduction & Basic Definitions **No. of Hours: 10**

History pf robots-robot anatomy, Coordinate Systems, Human arm Characteristics , Cartesian, Cylindrical, Polar, coordinate frames , mapping transform.

UNIT II: Kinematics – Inverse Kinematics **No. of Hours: 10**

Kinematics , Mechanical structure and notations , description of links and joints, Denavit Hatenberg notation , manipulator transformation matrix , examples inverse kinematics, 2D and 3D Robots.

UNIT III: Differential Motion – Statics – Dynamic Modeling **No. of Hours: 09**

Velocity Propagation along links, manipulator Jacobian – Jacobian singularities – Lagrange Euler formulation Newton Euler formulation basics of trajectory planning.

UNIT IV: Robot Systems **No. of Hours: 08**

Actuators Sensors and Vision: Hydraulic and Electrical Systems Including Pumps, valves, solenoids, cylinders, stepper motors, Encoders and AC Motors Range and use of sensors, Microswitches, Resistance Transducers, Piezo-electric, Infrared and Lasers Applications of Sensors: Reed Switches, Ultrasonic, Barcode Readers and RFID – Fundamentals of Robotic vision.

UNIT V: Robots and Applications: **No. of Hours: 08**

Industrial Applications – Processing applications – Assembly applications, Inspection applications, Non Industrial applications, Under water exploration and Space Exploration.

Textbooks:

1. Robotics and Control : R.K. Mittal and I.J. Nagarath, TMH 2003.
2. Introduction to Robotics – P.J. Mckerrow, ISBN: 0201182408

Reference Books:

1. Robotics – K.S. Fu, R.C. Gonzalez and C.S.G. Lee, 2008, TMH.
2. Introduction to Robotics – S. Nikv, 2001, Prentice Hall,

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(24MTME01Ta) INDUSTRIAL SAFETY

(Common to SE, ES, VLSID, CSE)

Course Objectives:

- To know about Industrial safety programs and toxicology, Industrial laws, regulations and source models
- To understand about fire and explosion, preventive methods, relief and its sizing methods.
- To analyse industrial hazards and its risk assessment.

Course Outcomes:

After completion of the course, the student should be able to:

CO1. Identify causes and types of accidents, its preventive steps, important legislations related to health, Safety and Environment. (L2)
CO2. Understand about various maintenance engineering methods, maintenance tools, its cost and life. requirements mentioned in factories act for the prevention of accidents. (L2)
CO3. Discuss types of Wear and Corrosion, their reduction techniques. (L2)
CO4. Understand about various types of Fault tracing methods. (L2)
CO5. Recognize necessity of various preventive maintenance strategies of mechanical and electrical equipment. (L2)

UNIT I: **No. of Hours: 09**

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

UNIT II: **No. of Hours: 09**

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relation with replacement economy, Service life of equipment.

UNIT III: **No. of Hours: 09**

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants- types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

UNIT IV: **No. of Hours: 08**

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine

tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

UNIT V: **No. of Hours: 10**

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

Textbooks:

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.

Reference Books:

1. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
2. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

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II Year I Semester

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(24MTCS02Ta) BUSINESS ANALYTICS

(Common to SE, ES, VLSID, CSE)

Course Objectives:

- The main objective of this course is to give the student a comprehensive understanding of business analytics methods.

Course Outcomes:

After completion of the course, the student should be able to:

CO1. Demonstrate knowledge of Business and data analytics. (L2)
CO2. Demonstrate the ability to think critically in life cycle systems. (L2)
CO3. Analyze the overview of requirements from different sources and their relationships by flow charts and flow diagrams. (L4)
CO4. Understand about types of requirements, acceptance, and requirements tools (L2)
CO5. Know the recent trends in Embedded and collaborative business intelligence (L2)

UNIT I: **No. of Hours: 09**

Business Analysis: Overview of Business Analysis, Overview of Requirements, Role of the Business Analyst.

Stakeholders: the project team, management, and the front line, Handling Stakeholder Conflicts.

UNIT II: **No. of Hours: 08**

Life Cycles: Systems Development Life Cycles, Project Life Cycles, Product Life Cycles, Requirement Life Cycles.

UNIT III: **No. of Hours: 10**

Forming Requirements: Overview of Requirements, Attributes of Good Requirements, Types of Requirements, Requirement Sources, Gathering Requirements from Stakeholders, Common Requirements Documents. Transforming Requirements: Stakeholder Needs Analysis, Decomposition Analysis, Additive/Subtractive Analysis, Gap Analysis, Notations (UML & BPMN), Flowcharts, Swim Lane Flowcharts, Entity-Relationship Diagrams, State-Transition Diagrams, Data Flow Diagrams, Use Case Modeling, Business Process Modeling

UNIT IV: **No. of Hours: 09**

Finalizing Requirements: Presenting Requirements, Socializing Requirements and Gaining Acceptance, Prioritizing Requirements. Managing Requirements Assets: Change Control, Requirements Tools.

UNIT V: **No. of Hours: 09**

Recent Trends in: Embedded and collaborative business intelligence, Visual data recovery, Data Storytelling and Data Journalism.

Textbooks:

1. Business Analysis by James Cadle et al.
2. Project Management: The Managerial Process by Erik Larson and, Clifford Gray

Reference Books:

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

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(24MTME01Tb) WASTE TO ENERGY

(Common to ES, VLSID)

Course Objectives:

- Introduce and explain energy from waste, classification and devices to convert waste to energy.
- To impart knowledge on biomass pyrolysis, gasification, combustion and conversion process.
- To educate on biogas properties, bio energy system, biomass resources and their classification and biomass energy programme in India.

Course Outcomes:

After completion of the course, the student should be able to:

CO1. Understand the concept of waste to Energy, classification of waste and waste to energy conversion devices. (L2)

CO2. Describe Biomass pyrolysis, manufacturing methods of charcoal, pyrolytic oils and gases. (L2)

CO3. Explain the construction and operation of various types of Biomass Gasifiers. (L2)

CO4. Operate and use various types of Biomass Combustors. (L2)

CO5. Discuss the properties of Biogas, various Biomass conversion process and Biogas plant technology. (L2)

UNIT I: **No. of Hours: 10**

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors.

UNIT II: **No. of Hours: 10**

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

UNIT III: **No. of Hours: 08**

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic consideration in gasifier operation.

UNIT IV: **No. of Hours: 09**

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

UNIT V: **No. of Hours: 08**

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification- pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants –

Applications - Alcohol production from biomass - Bio diesel production - Urban waste to energy conversion - Biomass energy programme in India.

Textbooks:

1. Non-Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 2018.
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., TMH, 2017.

Reference Books:

1. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
2. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley & Sons, 1996

Online Learning Resources:

https://nptel.ac.in/noc/courses/noc19/SEM1/noc19-ch13/

https://www.youtube.com/watch?v=x2KmjbCvKTk