Chief Patron
Sri MANNEM RAMI REDDY, MA., HDC.
Ex-EC Member, SVU Tirupati, Chairman, SRET
Patrons
Sri M. RAMA SUBBA REDDY BE, MBA (UK)
Secretary, SRET
Sri M. ARAVIND KUMAR REDDY BE, M.Tech., MBA(UK)
Director, SRET
Co-Patrons
Dr. K. JAYACHANDRA M.Tech., PhD
Principal, SRET
Dr. N. VASU M.Tech., PhD
Vice Principal, SRET
Coordinator:
Dr. R. NAGENDRA
Associate Professor & HOD of ECE
Sree Rama Engineering College, Tirupati
Email: hod.ece@sreerama.ac.in
Mobile: 9949632049
Co-Coordinator:
Dr. S. SRUTHI
Associate Professor, Department of ECE
Sree Rama Engineering College, Tirupati
Email: dr.sruthiece@gmail.com
Mobile: 7989532664

ORGANIZING COMMITTEE:

Dr. B. PRABHAKAR REDDY Professor, Department of ECE, SRET
Dr. M. HEMALATHA Professor, Department of ECE, SRET
Dr. A. RAJAN Professor, Department of ECE, SRET
Dr. B BHARATHIDASAN Professor, Department of ECE, SRET
Dr. SRIMATHI SEKHAR Professor, Department of ECE, SRET
Dr. B. LALITHA Associate Professor, Department of ECE, SRET
Mr. P. GIRI BABU Assistant Professor, Department of ECE, SRET
Mr. A. BALACHANDRA REDDY Assistant Professor, Department of ECE, SRET
Mr. S. CHAKRISREEDHAR Assistant Professor, Department of ECE, SRET
Mr. D. POORNACHANDRA REDDY Assistant Professor, Department of ECE, SRET
Mr. D. NAGENDRA BABU Assistant Professor, Department of ECE, SRET
Mrs. KOMALA DEVI Assistant Professor, Department of ECE, SRET
Mr. T. RAVISEKHAR Assistant Professor, Department of ECE, SRET
Mr. B. MURALIDHAR NAICK Assistant Professor, Department of ECE, SRET
Mrs. M. RAJESWARI Assistant Professor, Department of ECE, SRET
Ms. S. JAMEELA Assistant Professor, Department of ECE, SRET
Mr. B. SREENIVASAN Assistant Professor, Department of ECE, SRET
Mrs. B. SUNEETHA Assistant Professor, Department of ECE, SRET
Mrs. K. YOGITHA BALI Assistant Professor, Department of ECE, SRET
Mrs. B NAGATEJASWINI Assistant Professor, Department of ECE, SRET
Mr. M. VENKATA SUBBAIAH Associate Professor, Department of ECE, SRET

TECHNICAL COMMITTEE

Dr. D N SANDEEP Associate Professor, Department of ECE, SRET
Mr. K MADHU BABU Assistant Professor, Department of ECE, SRET
Mr. G K RAMMOHAN Assistant Professor, Department of ECE, SRET
Mr. S ROHITH Assistant Professor, Department of ECE, SRET
Mr. T PRAVEEN KUMAR Assistant Professor, Department of ECE, SRET
Mr. T JAYAKRISHNA Assistant Professor, Department of ECE, SRET
Mrs. G NIHARIKA Assistant Professor, Department of ECE, SRET
Mr. P SREEKANTH Assistant Professor, Department of ECE, SRET

REGISTRATION COMMITTEE

Mr. S NARENDRA Assistant Professor, Department of ECE, SRET
Mrs. N LAKSHMI Assistant Professor, Department of ECE, SRET
Ms. R V LOKESWARI Assistant Professor, Department of ECE, SRET
Mrs. DIVYA Assistant Professor, Department of ECE, SRET
Mr. G DEEPIKA Assistant Professor, Department of ECE, SRET

COORDINATION COMMITTEE

Mrs. M GURUSRAVYASREE Assistant Professor, Department of ECE, SRET
Mrs. B MOUNIKA Assistant Professor, Department of ECE, SRET
Mrs. T SARITHA Assistant Professor, Department of ECE, SRET
Mrs. P SUDHESHNA Assistant Professor, Department of ECE, SRET

FEEDBACK AND ASSESSMENT COMMITTEE

Mr. M RAJA MOHAN REDDY Assistant Professor, Department of ECE, SRET
Ms. N SWETHA Assistant Professor, Department of ECE, SRET
Mr. K MANIKANTA Assistant Professor, Department of ECE, SRET
Mr. K KUMAR CHAITANYA Assistant Professor, Department of ECE, SRET

Schedule:

Date	Time	Details of the session	Name of the Expert
Day 1 08.09.2025 Monday	6:00PM to 6:30PM	Inauguration	
	Session 1: 6.30 PM to 8.00 PM	Topic: Design of VLSI Architectures of cost quantum algorithms	Dr. P. Vikram Kumar, Associate Professor, Dept. of Electrical Engineering, IIT Tirupati
	Session 2: 8.00 PM to 9.30 PM	Topic: From Transistor to Chips: Exploring the Role of MOSFETs in VLSI Systems	Dr. Sivasubramanyam Medasani, Senior consultant (Electronics & VLSI), Symbiomics Technologies Private Limited, Ganesh Nagar, Kurnool
Day 2 09.09.2025 Tuesday	Session 3: 6.00 PM to 7.30 PM	Topic: RISC-V-Based System Design with AI-enabled Co Processors	Dr. B. Naresh Kumar Reddy Assistant Professor, Dept. of ECE, NIT Trichy
	Session 4: 7.30 PM to 9.00 PM	Topic: Designing high speed and low power ASICs using scalable memory compilers	Mr. P Veerendra Reddy, Senior manager-IP applications, Alphawave semi private Ltd, Bellandur, Bengaluru.
Day 3 10.09.2025 Wednesday	Session 5: 6.00 PM to 7.30 PM	Topic: Integrating VLSI with industry 4.0: A new era of smart Manufacturing	Dr. B. Chandrababu Naik, Assistant Professor, Dept. of ECE, NIT Trichy
	Session 6: 7.30 PM to 9.00 PM	Topic: AI Application in Design for Testability	Mr. V R Pradeep Bharadwaj Senior Manager-DFT, Synopsys India pvt. Ltd, Bengaluru
Day 4 11.09.2025 Thursday	Session 7: 6.00 PM to 7.30 PM	Topic: Nanoscale Semiconductor Devices: Low Power Applications	Dr. Ekta Goel, Assistant Professor, Dept. of ECE, NIT Warangal
	Session 8: 7.30 PM to 9.00 PM	Topic: From Code to Silicon: AI Powered revolution in RTL Design workflows	Dr.Shanmuga kumar Muragesan Founder & CEO, Modern Agriculture Technology Innovation Center (MATIC), Chennai
Day 5 12.09.2025 Friday	Session 9: 6.00 PM to 7.30 PM	Topic: Applications of Artificial Intelligence tools in VLSI Design	Mr. Avinash Yadlapati VLSI Design Engineer & Manager Altera, Penang, Malaysia
	Session 10: 7.30 PM to 9.00 PM	Topic: AI/ML for VLSI Design	Dr. Sk. Noor Mohammad, Associate Professor, Dept. of Computer Science and Engineering, IIITDM Kancheepuram,
Day 6 13.09.2025 Saturday	Session 11: 2.00 PM to 3.30 PM	Topic: Low Power VLSI Design for AI & Edge computing	Mr. Nimit Gandhi Staff Engineer, Lattice Semiconductor, Penang, Malaysia
	Session 12: 3.30 PM to 5.00 PM	Topic: Advanced FPGA Techniques: Reconfiguration, Timing and AI acceleration	Mr. PVSR Bharadwaja FPGA Design Engineer, Granite River Labs Technologies Pvt. Ltd., Bengaluru.
	Session 13: 5.00 PM to 6.30 PM	Topic: Open source EDA with AI integration	Mr. M Dhayala Kumar Director & CEO, Meister Gen Technologies Pvt. Ltd., Chennai
	6:30 PM to 7:30 PM	Online test & feedback	
	7:30 PM to 8:00 PM	Valedictory Session	

Note: No Registration fee for participants
Registration Link: https://atalacademy.aicte-india.org/login
NOC Form : https://sreerama.ac.in/srec/wp-content/uploads/2025/07/NOC-FDP.pdf

An AICTE Training and Learning (ATAL) Academy Sponsored
Online 6 Days Faculty Development Program (FDP)
On

INTELLIGENT VLSI DESIGN AUTOMATION USING AI TECHNIQUES

Organized by

Department of Electronics & Communication Engineering

08th to 13th September 2025

SREE RAMA ENGINEERING COLLEGE
(AUTONOMOUS)
Approved by AICTE, New Delhi – Affiliated to JNTUA, Ananthapuramu
Accredited by NAAC with 'A' Grade
Rami Reddy Nagar, Karakambadi road,
Tirupati-517507

About the College:

Sri Mannem Rami Reddy garu, the founder of Sree Rama Educational Society started SREE RAMA ENGINEERING COLLEGE (SRET) with an aim to impart quality education to the student community of backward region of Rayalaseema in the year 2008. His outstanding personality, acumen and magnificent vision have made him a benevolent patron of the institutions. We are very much pleased to introduce ourselves as one of the upcoming Engineering Colleges aspiring to provide high standards of technical education. SRET fosters a vision of educational transformation in keeping pace with the times. It emphasizes a symbiotic relationship among the students, faculty, academic curriculum and industries. The institution offers a holistic approach to technical education, personality development and soft skills.

Sree Rama Engineering College was started with an annual intake of 240 students in 4 branches. At present, the college offers 7 B.Tech programmes and 4 M.Tech. Programmes. The institute offers MBA programme as well. This educational institution aims to provide an academically exhilarating environment allowing the students to enjoy a first class education and social experience. Our college has accredited by NAAC with 'A' grade and NBA. The college has conferred with autonomous status by University Grants Commission (UGC) for a period of Ten years from 2024-25 to 2033-34.

About the ECE Department:

The Department of Electronics and Communication Engineering (ECE) was established in the year 2008 and has since evolved into a center of academic excellence. The department has a team of well-qualified, dedicated, and experienced faculty who guide students through the diverse and dynamic landscape of ECE. This discipline encompasses a wide range of subjects including analog and digital electronics, communication systems, VLSI design, embedded systems, signal processing and microwave engineering. The present intake of students for B.Tech. Program is 240. The department is equipped with well-established labs that give hands-on practical knowledge in the subjects. The laboratories are well equipped and sufficiently staffed for the applications of the theories to satisfy the curiosity of the students. To ensure a strong practical foundation, the department is equipped with eight state-of-the-art laboratories, including analog and digital electronics lab, communications lab, microprocessors and microcontrollers lab, VLSI and embedded systems lab and digital signal processing lab. The department initiates all student chapter activities of the Institution of Electrical and Electronics Engineers – IEEE, which is a global authority on the standardization of all aspects of Electrical and Electronics Engineering.

Department Vision:

To be a center of excellence in Electronics and Communications committed to advancing knowledge and research to develop high-caliber engineering professionals and entrepreneurs with strong ethical values, equipped to meet both local and global challenges

Department Mission:

M1. Impart knowledge through a contemporary curriculum, fostering growth and inclusivity among students from diverse backgrounds.

M2. Enhance students' employability by developing practical skills through a comprehensive training process

M3. Inspire students and faculty to pursue innovative research, building strong partnerships with research organizations and industry to address societal needs

M4. Instill ethics and values in students, ensuring responsible and impactful engineering practices.

About the FDP:

Integrating Artificial Intelligence techniques into VLSI design automation is transforming how integrated circuits are conceived, optimized and verified. AI empowers design engineers to automate complex tasks like logic synthesis, placement, routing and timing analysis with improved accuracy and efficiency. This convergence of AI and VLSI enhances scalability, reduces design cycles and facilitates intelligent decision-making in chip development. AI models help predict design bottlenecks, optimize power and area, and adaptively tune parameters throughout the EDA workflow. This FDP will provide insights into these innovations, equipping participants to adopt AI-driven tools in VLSI education, research and industry practice:

- AI automates and enhances VLSI design processes like synthesis, placement, routing, and verification, improving speed and precision.
- Machine learning models predict design issues and optimize performance, power and area in complex chip architectures.
- AI enables adaptive design space exploration and shortens development cycles, especially in advanced semiconductor nodes.
- Intelligent algorithms assist in fault detection, yield prediction, and reliability enhancement during IC development.
- AI processes vast amounts of data from smart meters, sensors and other sources to provide insights into energy consumption patterns, grid performance and infrastructure health, enabling informed decision-making.
- AI-based EDA tools improve productivity and allow designers to handle increasing design complexity with ease.
- The FDP explores cutting-edge AI techniques, datasets and tools that are reshaping modern VLSI design methodologies.

At the outset, artificial intelligence techniques play a pivotal role in shaping the future of VLSI design automation, making it more intelligent, efficient and sustainable.

Objectives of FDP:

The objectives of a faculty development program on the integration of artificial intelligence techniques in VLSI design automation include:

- Provide a multidisciplinary platform for faculty, researchers, and professionals in VLSI, electronics, computer science, and AI.
- Bridge the gap between traditional VLSI practices and modern AI-driven design automation techniques.
- Build strong conceptual understanding of integrating AI into VLSI design automation phases such as logic synthesis, floor planning, placement, routing, timing analysis and verification.
- Highlight the role of intelligent algorithms in enhancing design efficiency, accuracy, and scalability.
- Promote outcome-based education and support Curriculum Innovation aligned with technological trends.
- Empower faculty to modernize teaching practices and engage in advanced research.
- Encourage interdisciplinary collaboration by combining Electronics, Data Science, and Computational Intelligence.
- Provide training on effective pedagogical strategies and instructional methods for teaching AI concepts and applications

Outcome of the FDP:

After completion of this FDP, the Faculty will have to

- Enhance understanding of the principles and applications of artificial intelligence in the context of VLSI design.
- Improve ability to design an energy-efficient, high-performance integrated circuit.
- Carry out Interdisciplinary collaboration among electronics, computer science and data science domains.
- Contribute towards building a dynamic academic and research ecosystem in the field of intelligent VLSI design.
- Conduct Research and Development activities in the field of AI-enabled VLSI.
- Strengthen collaboration and networking among faculty members and industry experts for knowledge sharing and interdisciplinary research.
- Educate and mentor students in the emerging field of AI driven VLSI.
- Align curriculum and teaching methodologies with the latest advancements in AI and its integration in VLSI design.
- Establish partnerships and collaborations with industry stakeholders for technology transfer and commercialization of AI solutions in the VLSI domain.
- Support national goals in semiconductor innovation and enhance global competitiveness in microelectronics.

Targeted Participants:

The faculty members of the AICTE approved institutions, Research Scholars, PG Scholars, and participants from Government, Industry Bureaucrats / Technicians / Professionals / School Teachers and Staff of Host institutions.

Merit Certificates to Participants:

A test will be conducted by the Program Evaluation Committee (PEC) at the end of the program and the e-certificates will be issued to those participants who have attended all the sessions of the program and have qualified in the test.