ATAL Online 6 Day Faculty Development Programme 2025-26 Schedule

FDP Thrust Area: Semiconductors

FDP Title: Intelligent VLSI Design Automation using AI Techniques

Start Date: 08/09/2025 **End Date: 13/09/2025**

Day 1 (08/09/2025)	Day 2 (09/09/2025)	Day 3 (10/09/2025)	Day 4 (11/09/2025)	Day 5 (12/09/2025)	Day 6 (13/09/2025
6:00PM to 6:30PM	6:00PM to 7:30PM	6:00PM to 7:30PM	6:00PM to 7:30PM	6:00PM to 7:30PM	2:00PM to 3:30PM
Inaugural Session	**Session 3**	**Session 5**	**Session 7**	**Session 9**	**Session 11**
	Topic: RISC-V-Based System Design with AI-enabled Co-Processors **Name of the Expert:** Dr. B. Naresh Kumar Reddy **Designation & Organization:** Assistant Professor, Department of ECE, NIT Trichy **Years of Exp:** 10 years	**Topic:** Integrating VLSI with industry 4.0: A new era of smart Manufacturing **Name of the Expert:** Dr.B. Chandrababu Naik, **Designation & Organization:** Assistant Professor, Department of ECE, NIT Trichy **Years of Exp:** 13 years	**Topic:** Nanoscale Semiconductor Devices: Low Power Applications **Name of the Expert:** Dr. Ekta Goel, **Designation & Organization:** Assistant Professor, Department of ECE, NIT Warangal **Years of Exp:** 10 years	**Topic:** Applications of Artificial Intelligence tools in VLSI Design **Name of the Expert:** Mr. Avinash Yadlapati **Designation & Organization:** VLSI Design Engineer Manager Altera, Penang Malaysia **Years of Exp:** 22 years	**Topic:** Low Power VLSI Design for AI & Edge computing **Name of the Expert:** Mr. Nimit Gandhi Staff Engineer, Lattice Semiconductor, Penang, Malaysia **Years of Exp:** 10 years
6:30PM to 8:00PM	7:30PM to 9:00PM	7:30PM to 9:00PM	7:30PM to 9:00PM	7:30PM to 9:00PM	3:30PM to 5:00PM
Session 1	**Session 4**	**Session 6**	**Session 8**	**Session 10**	**Session 12**
Topic: Design of VLSI Architectures of cost quantum algorithms **Name of the Expert:** Dr. P. Vikram Kumar **Designation & Organization:** Associate Professor, Department of Electrical Engineering, IIT Tirupati **Years of Exp:** 11 years	**Topic:** Designing high speed and low power ASICs using scalable memory compilers **Name of the Expert:** Mr. P Veerendra Reddy, **Designation & Organization:** Senior manager-IP applications, Alphawave semi private Ltd, Bellandur, Bengaluru. **Years of Exp:** 14 years	**Topic:** AI Application in Design for Testability **Name of the Expert:** Mr. V R Pradeep Bharadwaj **Designation & Organization:** Senior Manager-DFT, Synopsys India pvt. Ltd, Bengaluru **Years of Exp:** 14 years	**Topic:** From Code to Silicon: AI-Powered revolution in RTL Design workflows **Name of the Expert:** Dr. Shanmugakumar Muragesan **Designation & Organization:** Founder & CEO, Modern Agriculture Technology Innovation Center (MATIC), Chennai **Years of Exp:** 12 years	**Topic:** AI/ML for VLSI Design **Name of the Expert:** Dr. Sk. Noor Mohammad, **Designation & Organization:** Associate Professor, Department of Computer Science and Engineering IIITDM Kancheepuram, **Years of Exp:** 20 years	**Topic:** Advanced FPGA Techniques: Reconfiguration, Timing and AI acceleration **Name of the Expert:** Mr. PVSR Bharadwaja, **Designation & Organization:** FPGA Design Engineer, Granite River Labs Technologies Pvt. Ltd., Bengaluru. **Years of Exp:** 11 years
8:00PM to 9:30PM					5:00PM to 6.30PM
Session 2					**Session 13**
Topic: From Transistor to Chip: Exploring the Role of MOSFETs in VLSI Systems **Name of the Expert:** Dr. Sivasubramanyam Medasani, **Designation & Organization:** Senior consultant (Electronics & VLSI), Symbiomics Technologies Private Limited, Ganesh Nagar, Kurnool **Years of Exp**: 12 years					**Topic:** Open source EDA with AI integration **Name of the Expert:** Mr. M DhayalaKumar Director & CEO, Meister Gen Technologies Pvt. Ltd., Chennai **Years of Exp:** 11 years
					6:30PM to 7:30PM Online test & feedback
					7:30PM to 8:00PM Valedictory Session